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Voltage Stability Improvement Using Series FACTS Devices

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Abstract: In this paper, voltage stability assessment with appropriate representations of the FACTS series devices is investigated and compared in the modified IEEE 14-bus test system. The target function to determine the TCSCs installing place is increasing voltage stability during fault occurrence. By determining TCSCs optimum installation place, their success rate buses voltage stabilization is studied by a new following index named voltage stability index, and it is presented that TCSCs can be considerably successful in voltage stability during fault contingency. TCSC installation effect on amount of load shedding reduction is also presented as a new subject to keep buses voltage stability.

Key words: Thyristor controlled series capacitor (TCSC), TCSC allocation, fault contingency, voltage buses stability, load shedding

INTRODUCTION

Power system as a large scale system is always under various faults. A great part of these faults is related to connection of transmitting lines. These faults can lead lines to outage which causes two following main problems:

1. Overload creation in other correct lines.
2. Voltage unstable conditions in system buses.

In order to decrease mentioned problems, various methods are presented and Thyristor controlled series capacitor as a FACTS device is one of them. This system generally is used to create a controlled series capacitor in lines (Gama and Tenorio, 2002). Thyristor controlled series capacitor can increase lines and buses voltage stability domain by fast impedance control of lines during power system ordinary work (Huang and Nair, 2002), (Kamarposhti and Alinezhad, 2009), (Laifa and Boudour, 2009).

It is necessary to mention that, TCSC effect on increasing the voltage static stability in system's ordinary operation point is an accepted issue, but the study of TCSC effect on the above issues during fault contingency conditions can be interesting (He *et al*, 1999). It seems that TCSC can also be applied to reduce above problems during fault contingency because of its high operation speed and lines inductive reactance reduction. In order to optimum use of TCSC in power system, it is necessary to initially recognize the best point of their installation and make sure that their operation is not under not optimized installation effect (Shizawa *et al*, 2004),(Yorino *et al*, 2004). In this paper a new method is presented to optimum TCSC allocation in an associated power system which is a kind of sensitivity analysis method. It should be noted that since we assume no limit in used TCSCs and more important than that because of real power systems expansion, TCSCs optimum installing location is time consuming by using methods like try and error and so an appropriate method is necessary to determine TCSC optimum installing place. For example, in order to two different TCSCs with different values in a IEEE 14 bus power system which has 20 transmitting lines, the studied conditions, by applying mentioned methods and assuming that the TCSCs are not located on a single line will be19^{20} conditions.

Also in this paper, by presenting new numerical indexes it is shown that TCSC is very effective to stabilize buses voltage during fault contingency.

MATERIALS AND METHODS

This paper is consisted of four main parts. First of all, this paper investigates the TCSC Optimum Allocation in section I. Then, Applying Proposed Method in IEEE 14 Bus System is presented in section II. Modeling Applying Proposed Method in IEEE 30 Bus System is presented in section III and TCSC Efficiency in Buses Voltage Stability during Fault Contingency is presented in section IV.

I. TCSC Optimum Allocation:

In order to study TCSC efficiency in reducing lines overload and buses voltage stabilization the best point

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of TCSC installation should be determined at the first stage. In this part, a method is presented to achieve this aim. The main idea of suggested optimum allocation method is defining an index named Single Contingency Sensitivity (SCS) to each line. This method is based on the transmitting lines sensitivity analysis related to different faults. This index is used to select the best place of TCSC installation. It should be mentioned that, if places defined for TCSC are optimized to reduce lines overload, these places would be optimized for bus voltages. The reason is that, as the P-V characteristics in power buses, the line under more overload during different fault conditions, will create a sever voltage unstable condition probability if it outages the system (Eidiani, 2010),(Zare, 2009). SCS_j coefficient which is defined by relation (1) shows the sum of j^{th} line normalized overload caused by m faults leading the j^{th} line overload.

$$SCS_j = \sum_{i=1}^{m} P_i U_{ij} W_{ij} \tag{1}$$

It should be noted that if power system has n transmitting lines, fault contingency in all of them will not lead to overload in j^{th} line necessarily and generally just m faults may increase j^{th} line overload to more than the maximum transmittable load. It is obvious that m can be equal to or less than n.
Relation (1) also considers the i^{th} line outage probability (P_i) according to system background. Also, it is assumed that the system lines have single contingency outage and two lines never outage at the same time. The used matrixes and arrays applied for this issue are defined as follow:

U Matrix:

m×n binary matrix whose elements are "1" or "0". Each row of this matrix shows a specific fault. For example if (i) faults occur in transmitting system, elements in i^{th} row whose related transmitting line is overloaded under effect of this fault will obtain the value of "1" and naturally other elements of this row will obtain "0" value. It is obvious that the aim of defining this matrix is making j^{th} line SCS index zero which dose not overload if (i) circumstance occurs.

W Matrix:

An m×n matrix that normalizes overload value of the lines overloaded during fault contingency. Actually this matrix determines the lines overload value. j^{th} line's normalized load distribution under (i) circumstance is obtained by relation (2) as following:

$$\frac{P_{ij,cont.}}{P_{oj,nor.}} - 1 \tag{2}$$

Where $P_{ij,cont}$ and $P_{og,nor}$ respectively are the j^{th} line transmitted power in i^{th} line outage and ordinary work.

P Circumstance Probability Array:

This array is an m×1 array. In this array the probability of lines outage is computed by system's background information.

$$P_{m*1} = [P_1, P_2, ...P_m]^T \tag{3}$$

After computing different lines SCS, the lines are classified upon their SCS values. The line with the least SCS is the best place to install TCSCs, because in compare with the other lines, there is it has overloading probability during fault contingency condition and thus by installing TCSC on this mentioned line and reducing induction reactance of it, we can increase the load amount and the overload of other lines towards this line. (It is obvious that if we consider only the induction domain of TCSC the classification arrange will be changed). TCSCs locations are determined according to the lines rankings and the number of TCSCs which should be installed. Suggested TCSC optimum allocation method steps are as follow:

1. Refer to studied system's background and determine outages of each power system line to define P array elements.
2. Exploitation experiments in more appropriate lines (such as the lines with higher voltage levels) are determined to limit seeking domain.
3. U and W matrixes and arrays are composed and transmitted power in system's ordinary work is obtained. In this paper 1.2 times of line transmitting power is considered as its maximum transmittable power.
4. Each line's SCS is computed by relation 1.
5. First and second TCSCs are placed in obtained places upon mentioned classification but it should be noted that the rest of them should not be placed on the line which forms a loop with others and if so, TCSC is installed on the next ranked line.

For more clarification, we use IEEE 14 and 30 bus systems as the studied systems and obtain the optimum location of TCSC capacitors in them. Assume that the TCSC can change from zero to 50% of considered line impedance.

Considering the grid construction in our studies is the reason of applying two systems.

II. Applying Proposed Method in IEEE 14 Bus System:

IEEE 14 bus system structure is shown in fig. 1 (Kodsi and Canizares, 2003). 1-2, 1-5, 2-3, 2-4, 2-5, 3-4, 4-5 lines are selected as the main candidates of TCSC installation places to limit the seeking domain. In this example all lines probability of outage are considered the same and equal to 0.05.

Lines SCS values and their rankings are shown in table 1. In respect to table 1, line 3-4 is the best place to install the first TCSC because it has the least SCS value. According to this table lines 2-3 and 1-2 are in the next ranks and next TCSCs can be installed on them.

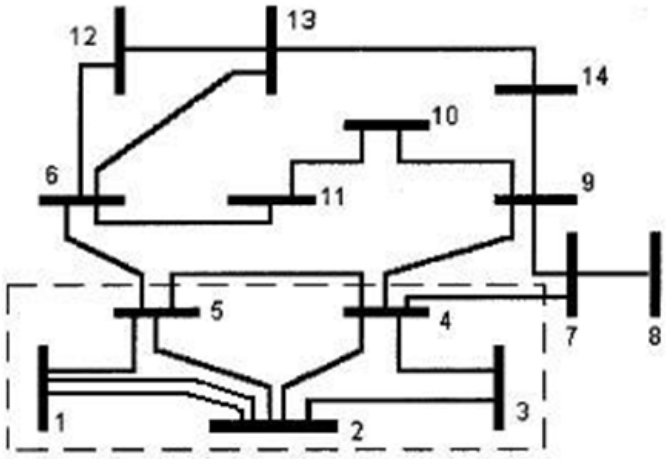

Fig. 1: IEEE 14 bus system structure.

Table 1: IEEE 14 bus Lines SCS values and their rankings.

Line	SCS value	Rating
1-2	0.0185	3
1-5	0.0198	4
2-3	00157	2
2-4	0.0414	5
2-5	0.0436	7
3-4	0.0030	1
3-5	0.0422	6

III. Modeling Applying Proposed Method in IEEE 30 Bus System:

In order to generalize the mentioned method, TCSC optimum allocation in IEEE 30 bus system is also applied. Fig. 2 shows this mentioned system. This system's lines outage probability with SCS values and their ranks are mentioned in table 2. According to this table we can see that the line 5-7 is the best place to install the first TCSC because of owning the least SCS in compare with the other lines.

Table 2: IEEE 30 bus Lines SCS values and their rankings.

Line	outage probability	SCS value	Rating
1-2	0.02	0.0383	5
1-3	0.03	0.0417	7
2-4	0.03	0.1395	12
3-4	0.03	0.0406	8
2-5	0.06	0.0404	6
2-6	0.06	0.1166	11
4-6	0.05	0.0749	9
5-7	0.05	0.0047	1
6-7	0.05	0.0049	2
6-8	0.04	0.0060	3
8-28	0.04	0.0176	4
6-28	0.04	0.1709	10

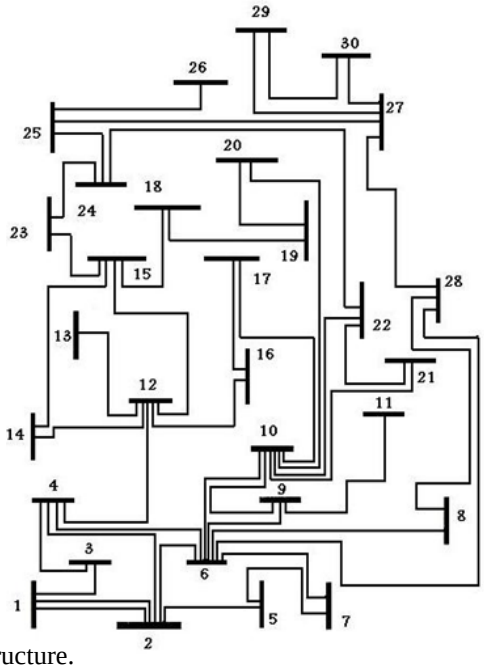

Fig. 2: IEEE 30 bus system structure.

IV. TCSC Efficiency in Buses Voltage Stability During Fault Contingency:

After optimum allocation of TCSCs using suggested method in part 2, in this part, TCSC efficiency in buses voltage stability during fault contingency is studied. In order to study this issue, an index named "voltage stability index" is defined and used. This index is defined by equation 4.

$$L_j = \left| \frac{\overline{S}_{j+}^{\,*}}{\overline{Y}_{jj} + \left| V_j^{\,2} \right|} \right| \tag{4}$$

where

$$\overline{S}_{j+} = \overline{S}_j + \overline{S}_{jcorr} \tag{5}$$

and

$$\overline{S}_{jcorr} = \left(\sum_{i \in l} \frac{Z_{ji}^{\,*}}{Z_{jj}^{\,*}} \times \frac{\overline{S}_i}{\overline{V}_i} \right) \overline{V}_j \tag{6}$$

Voltage stability index value will always fall between 0 and 1. zero means complete voltage stability and 1 means complete unstable voltage condition. Note that the maximum acceptable j^{th} bus amplitude is defined by $L_{j,crit}$ value. In fact this value shows the critical point of P-V curve for j bus.

$$L_j \le L_{j,crit.} \quad (7)$$

During fault contingency and line outage in a power system there is possibility for buses to get unstable or get close to such condition. In order to prevent this, two solution ways are considered as follow:

1. Shed or decrease the load of such buses.
2. TCSC allocation in the lines ending to these buses.

In this part it will be shown that the 2nd way is very effective and we can prevent unstable condition of system by applying TCSC without vast system vast shedding. In order to handle this study, IEEE 14 bus system is studied first and then IEEE 30 bus system is studied.

IEEE 14 Bus System:

In this system for example, 4 and 3 buses voltages are studied during lines 2-3 and 2-4 outage. The results of this study are brought in table 3.

According to the results of part 2, TCSC is placed in line 3-4 and provides the possibility of getting 35% impedance reduction. In 3rd column of this table, the voltages of mentioned buses are shown before fault, after fault without using TCSC and after fault using TCSC, respectively. In the next three columns of this table, the value of the voltage stability index of the related buses before fault, after fault without TCSC and after fault using TCSC are shown respectively. The last column shows the load value which should be shedded of the TCSCless system to reach the voltage stability value of it after fault contingency to the voltage stability index value of system using TCSC.

For example in first row, in ordinary work condition, bus 3 voltage stability index value is 0.1122. Now if the TCSC is not installed and for some reason 2-3 line does not outage then voltage value reaches to 0.1970 and if in TCSC installed condition 2-3 line outages, this value reaches to 0.1253. Note that, if we wanted to bring voltage stability index to 0.1253 without using TCSC we had to omit 46.8 MW load of bus 3 which is close to its half total load. We can understand that, TCSC can greatly be helpful to increase buses voltage stability and to reduce load shedding.In order to be surer about the results, IEEE 30 bus system is studied as a sample system too.

Table 3: Bus voltage of IEEE 14 bus standard system in various conditions.

Bus number	outage	Bus Voltage before fault (pu)	Bus Voltage after fault (pu)		L_j before fault	L_j after fault		TCSC Installation line	(MW)Load Reduction
			without TCSC	with TCSC		without TCSC	with TCSC		
3	2-3	1.010	0.910	0.96	0.1121	0.1970	0.1256	3-4	48.5
4	2-4	1.016	0.941	1.01	0.0391	0.0438	0.0412	3-4	6.2

IEEE 14 Bus System:

In this sample system, for example, bus 5 voltage is studied during line 2-5 outage. The results are registered in table 4. According to the results of part 2, TCSC is placed in line 5-7 and decreases 35% of its impedance. Bus 5 voltage stability index is 0.092 before fault contingency. This index is 1.19 and 1.05 after fault contingency for the cases with and without TCSC respectively. Now if we want to bring bus 5 voltage stability index to 1.05 in TCSCless mode, we have to decrease 27MW of its load. Results of studies on both sample systems obviously show that TCSC has a great efficiency in increasing buses voltage stability during fault contingency and line outages.

Table 4: Bus voltage of IEEE 30 bus standard system in various conditions.

Bus number	outage	Bus Voltage before fault (pu)	Bus Voltage after fault (pu)		L_j before fault	L_j after fault		TCSC Installation line	(MW)Load Reduction
			without TCSC	with TCSC		without TCSC	with TCSC		
5	2-5	1.010	0.940	0.968	0.092	0.119	0.105	5-7	27
7	6-7	1.003	0.958	0.980	0.083	0.109	0.097	5-7	4.8

Conclusion:

In this paper a new index named "voltage stability index" is used to study the TCSC efficiency in buses voltage stability during fault contingency. A new method is suggested to optimum allocation of TCSC. According to the results, TCSCs are greatly successful to increase buses voltage stability during fault contingency. On the other hand, results show that we can greatly reduce the amount of load shedding during fault contingency in order to keep the stability by installing TCSCs in optimum points.

REFERENCES

Eidiani, M., 2010. A New Method for Assessment of Voltage Stability in Transmission and Distribution Networks, International Review of Electrical Engineering (IREE). 5(1): 234-240.

Gama, C., R. Tenorio, 2002. Improvements for power systems performance: modeling, analysis and benefits of TCSC. IEEE Power Engineering Society Winter Meeting, 2: 1462-1467.

He, Y., P. Sicard, J. Xu, Z. Yao, V. Rajagopalan, 1999. A unified optimal controller design of TCSC to improve the power system dynamic stability. IEEE Power Engineering Society Winter Meeting, 1: 743-748.

Huang, G.M., N. K. Nair, C., 2002. Incorporating TCSC into the voltage stability constrained OPF formulation. IEEE Power Engineering Society Summer Meeting, 3: 1547-1552.

Kamarposhti, M., M. Alinezhad, 2009. Effects of STATCOM, TCSC, SSSC and UPFC on Static Voltage Stability, International Review of Electrical Engineering (IREE), 4(6): 1376-1384.

Kodsi, S.K.M. and C.A. Canizares, 2003. Modeling and simulation of IEEE 14 bus system with FACTS controllers, Technical report, University of Waterloo, Canada.

Laifa, A., M. Boudour, 2009. Multi-Objective Particle Swarm Optimization for FACTS Allocation to Enhance Voltage Security. International Review of Electrical Engineering (IREE), 4(5): 994-1004.

Shizawa, R., K. Nishida, T. Ohtaka, S. Iwamoto, 2004. Allocation of TCSC from transient stability view point. International Conference on Power System Technology, 216-221.

Yorino, N., E. El-Araby, H. Sasaki, S. Harada, 2004. A new formulation for FACTS allocation for security enhancement against voltage collapse, IEEE Transactions on power systems, 18(1): 3-10.

Zare, A., 2009. Evaluation Rating of Power Flow Based Voltage Stability Index, International Review of Modeling and Simulation (IREMOS), 2(6): 625-632.