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Static-Dynamic Full Adder Cell Based on a New Logic Approach

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Abstract: As full adder cells duplicate many times in arithmetic circuits, their power consumption is an important factor in total power consumption of the system. This paper presents a new full adder based on a new logic approach, which uses only one XNOR gate to implement 1-bit full adder cell. Using a novel XNOR gate and the new logic approach, a mixed static and dynamic 10-transitor (10T) full adder is implemented. Simulations have been carried out using HSPICE in 0.18 µm bulk technology. The results show that the 10T proposed full adder has less power delay product (PDP) in comparison to other simulated full adders.

Key words: Full adder. Low Power. Performance. Logic approach. CMOS VLSI.

INTRODUCTION

The Full adder is a fundamental design unit in various digital circuits, especially in circuits used for performing arithmetic operations such as compressors, comparators and parity checkers (Bui *et al.,* 2002) Thus, it is an important contributor to the overall power consumption of the large systems.

There are several issues related to the full adders. These include power consumption, performance, area, noise immunity, regularity, and good current drive capability (Ghadiry et al., 2010; 2011; 2011). Several works have been done to decrease transistor count and consequently decrease power consumption and area (Ghadiry *et al.,* 2009; Senejani *et al.,* 2009). They can broadly be categorized into full swing and non-full swing adders. Full swing full adders are normally robust with good properties in terms of power and speed (Goel *et al.,* 2006). However, they occupy large area (Bui *et al.,* 2002; Ghadiry *et al.,* 2011). Although non-full swing full adders normally suffer from threshold loss problem, they are useful in building up larger circuits such as multiple bit input adders and multipliers. One such established application is the Manchester carry-lookahead chain (MCC) (Bui *et al.,* 2002.

Proposed Xnor Circuit:

A new XNOR circuit has been implemented in a dynamic structure as shown in Fig. 1(a). A pass gate tree is used to implement the circuit in dynamic logic. Short circuit and leakage power are decreased due to use of no GND in the circuit. In addition, the circuit's speed is acceptable because of the high-speed nature of pass gates and dynamic logic used. The output is full swing between VDD and GND, which overcomes the threshold loss problem. However, using dynamic logic circuits causes problems when they are cascaded. As it will bee shown in Fig. 2, no dynamic circuit is used after this XNOR, thus the well-known problems associated with the dynamic circuits are avoided. However, clock load, complexity of design and testing are drawbacks of the proposed circuit. Fig. 1(b) shows the proposed 4-transistor dynamic XNOR circuit. Table I shows the operation of the circuit during the precharge and evaluation phases.

Table 1: Circuit operation and output voltages

Input CB	Pre Chrg. (clk=0)	Eval. (clk=1)
01	VDD	GND
10	VDD	GND
11	VDD	unchanged
00	VDD	unchanged

Mixed Dynamic and Static 10t Full Adder (Ds10t):

XOR or XNOR modules are the components that consume great deal of power in a full adder cell. As

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can be seen in Table II, COUT and SUM can be generated using intermediate signal $\overline{B \oplus C}$. The new logic approach reduces power consumption of the cell by decreasing the number of XOR or XNOR modules to one.

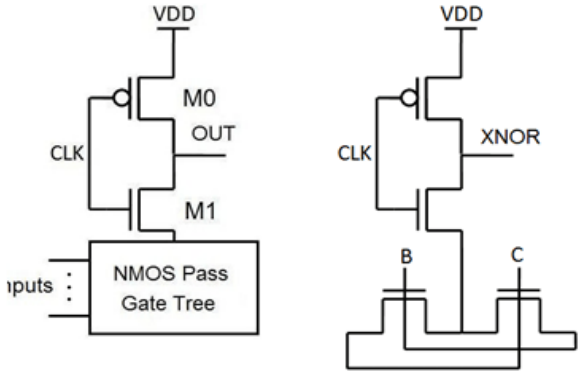

Fig. 1.(a): The proposed dynamic pass gate structure (b) The proposed dynamic full swing XNOR with four transistors.

Table 2: Truth table for the Proposed Structures

C	B	A	$\overline{B \oplus C}$	COUT	SUM
0	0	0	1	*C*	*A*
0	0	1	1	*C*	*A*
0	1	0	0	*A*	$\overline{A}$
0	1	1	0	*A*	$\overline{A}$
1	0	0	0	*A*	$\overline{A}$
1	0	1	0	*A*	*A*
1	1	0	1	*C*	*A*
1	1	1	1	*C*	*A*

The proposed circuit is shown in Fig. 2. In this circuit, using no GND connection results in low static power consumption. COUT and SUM generator circuits are two multiplexers that each uses only two transistors. Therefore, the proposed circuit uses only 10 transistors while it benefits from high-speed dynamic XNOR gate with full swing outputs. The ground connection in the inverter, which inverts input A has been removed in order to decrease more power consumption.

The main problem of the proposed full adder cell is the output threshold loss, which is equal to V_T.

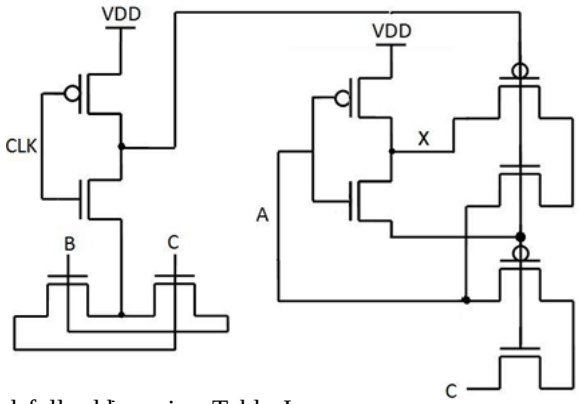

Fig. 2: DS10T proposed full adder using Table I

Simulation Setup:

All simulations have been carried out using HSPICE in 0.18 µm technology. In order to introduce more

realistic test environment two inverters have been used at the inputs. All outputs are connected to capacitive loads.

The performances of the circuits under test have been evaluated in term of worst-case propagation delay. Rise time and fall time of input signals are 5% of the input pulse width in all simulations. Transistors have been sized accordingly in order to minimize the PDP. Several input patterns were used to obtain average power consumption and worst-case delay in the circuit under test.

Results:

As Table III shows, the new design has improvement in terms of PDP over all simulated designs in 5 fF output load and 50 MHz operating frequency. In terms of power, it is better than Hybrid and complementary CMOS full adder (CCMOS), but not the transmission function full adder (TFA) and 16T at 1.8 V supply voltage. This is mainly because of the low swing output voltage of the proposed design, which causes high static power in cascaded mode. However, at 1.5 V, it is the lowest power-consuming circuit. In terms of delay, it is only second to Hybrid at 1.8 V.

Table 3: Simulation results at 1.8 V and 1.5 V

	Power (μW)		Delay (ns)		PDP (fJ)	
	1.8V	1.5V	1.8V	1.5V	1.8V	1.5V
This work	40.0	20	1.26	1.37	50	27
16T[7]	37.0	21	1.45	1.60	54	34
Hybrid[7]	42.1	24.4	1.22	1.33	51	32
CCOMS[7]	46.2	27.1	1.34	1.47	62	40
TFA[7]	35.7	20.3	1.46	1.64	52	33

Conclusion:

A new logic approach for designing a full adder cell was proposed which omitted XOR module against symmetric designs with XOR and XNOR modules. The proposed approach resulted in low power consumption compared to the existing full adder architectures. A new 4-bit adder was implemented based on the proposed logic and compared to several reported adder designs in the literature. Results show that it provides improvements in terms of power, delay, and PDP.

REFERENCES

Bui, H.T., Y.W. and Y. Jiang, 2002. *Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates.* IEEE Trans. Circuits Systems-II: Analog Digit. Signal Process, 49(1): 25-30.

Ghadiry, M.H., M. Nadisenejani and M. Miryahyaei, 2010. *A New full swing full adder based on a new logic approach.* World Applied Sciences Journal, 11(7): 808-811.

Ghadiry, M.H., Abu Khari A'Ain and M. Nadisenejani, 2011. *Design and analysis of a novel low PDP full adder cell* J. Circuits, Systems, and Computers, 20(3): 439-445.

Ghadiry, M.H., et al., 2011. *Design and Analysis of a New Carbone Nanotube Full Adder Cell.* J. of Nanomaterials, 2011(2011): 6.

Ghadiry, M.H., H. Mohammadi and M. Nadisenejani, 2009. *Two new low power high performance full adder with minimum gates.* Int. J. of Electrical and Information Engineering, 3(1): 124-131.

Goel, S., A., Kumar, M.A. Bayoumi, 2006. *Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style.* IEEE Trans. on VLSI Systems, 14(12): 309-1321.

Senejani, M.N., M.H. Ghadiry and M. Miryahyaei, 2009. *Low dynamic power high performance full adder*. in *Proc. of ICFCC.*