Design and Simulation of 5GHz Down-Conversion Self-Oscillating Mixer

1Alishir Moradikordalivand, 2Sepideh Ebrahimi and 3Mahmoud Abdipour

1Faculty of Electrical Engineering University Technology Malaysia.
2Young Researchers Club, Islamic Azad University, Aligodarz Branch, Aligodarz, Iran.
3Arak Islamic Azad university, Arak, Iran.

Abstract: In this paper a self-oscillating mixer is presented fundamental signal generated by the oscillator subcircuit in the mixing process. The oscillator core consumes 3 mA of current from a 1.8 V DC supply and results in an output power of -0.88 dBm per oscillator and a measured phase noise of -91, -102 and -107 dBc/Hz at 100 KHz, 600 KHz and 1 MHz from the carrier, respectively. In the mixing process the proposed mixer achieved IIP3 of 0 dBm with conversation gain of 1.93 dB. The circuit was designed and simulated in 0.18-μm CMOS technology by ADS2010.

Key words: Self-oscillating mixer (SOM), VCO, CMOS, Up-conversation Mixer.

INTRODUCTION

In modern microwave communication systems, low cost, small size and low power consumption circuits are required that combine multiple functions with a reduced number of components. For the realization of receiving systems, the harmonic self-oscillating mixer (SOM) is an attractive option (G.C. Wang et al., 1994; M.R. Tofighi and A.S. Daryoush, 2005; S.A. Winkler et al., 2007; F. Plessas et al., 2007; S. Ver Hoeye et al., 2011; L.F. Herrán et al., 2006) since a single transistor is employed to realize the local oscillator signal as well as a mixing operation between the input signal and a harmonic component of the self-oscillation. In harmonic balance (HB), several techniques have been presented for the nonlinear analysis and design of SOM-circuits (S. Ver Hoeye et al., 2011; L.F. Herrán et al., 2006). With these techniques the designer has an increased control over the SOM self-oscillating frequency, the harmonic content and the conversion gain. However, for the design of wide-band harmonic SOM circuits with high conversion gain, additional techniques are required.

A common problem referring to SOM solutions has been the Lack RF-to-local oscillator (LO) isolation emerging by the combination of the two circuit functions into one device. This problem has been addressed in numerous publications and a common solution to bypass this issue is given by the use of a dual-gate FET, using one port for the oscillation feedback network and injecting the RF input signal at the second port (J. Zhang et al., 1999; J. Xu and K.Wu, 2005; Y. Chen and Z. Chen, 2003). Another possibility to eliminate this problem is the use of a balanced circuit structure (Winkler, S.A. et al., 2006; Gook-Ju Ihm, 2004; Yuan-Kai Chu et al, 2003; Xuezhen Wang and Robert Weber, 2004), which offers inherent RF-LO isolation, as well as a number of other important advantages such as lower AM noise, suppression of unwanted harmonics, etc. Furthermore, the input does not have to be matched both at LO and RF frequencies, which simplifies the input matching requirements.

Efforts have been made to integrate SOMs with antennas to form receivers (J. Zhang et al., 1999; Y. Chen and Z. Chen, 2003; M. Tiebout and T. Liebermann). This allows for building a simple receiver circuit without the use of an input RF balun, as it would be required in conventional balanced mixers. Thus, the presented solution results in a planar design, which is highly desired in many commercial low-cost applications.

Design of a 5 GHz VCO:

The cross-coupled VCO is the most common microwave VCO topology used in CMOS technology. An LC VCO can be modeled with the capacitor and inductor in parallel with a resistor to model the losses in the tank as well as a negative resistance that models the active device. One way of generating the negative resistance to compensate for the losses in the LC tank is to use a cross-coupled differential pair as shown in Figure 1. The resistance, \( R_n \), looking into the cross-coupled pair is given by:

\[
R_n = \frac{2}{g_m}
\]
Where $g_m$ is the transconductance of each of the BJTs in the cross-coupled pair. Therefore, with an appropriate device size and biasing, the value of negative resistance required to counteract the losses in the tank can be realized.

![Negative resistance generated from cross-coupled BJT.](image1)

**Fig. 1:** Negative resistance generated from cross-coupled BJT.

A commonly used LC VCO circuit using the cross coupled differential pair is shown in Figure 2. In this implementation a relatively low supply voltage is possible since there are only two levels of transistors, but it requires two inductors, which can consume significant chip area.

The VCO topology shown in Figure 2 was used (with FET transistor) in (S. Ver Hoeye *et al.*, 2001).

![Cross-coupled BJT VCO.](image2)

**Fig. 2:** Cross-coupled BJT VCO.

In this work, CMOS 0.18 $\mu$m technology was used to design fundamental C band VCO. The Diode varactor shown in Figure 2 enables the frequency tuning. The signal output power was approximately -0.942dBm and the phase noise at a 1 MHz offset was -107.9dBc/Hz.

Figure 3 shows Graph of phase noise. Figure 4 shows spectrum of output power and figure 5 shows Time-domain VCO outputs.

![Phase noise 4.8GHz VCO.](image3)

**Fig. 3:** Phase noise 4.8GHz VCO.
Down-Conversion Self-Oscillating Mixer Design:

The single balanced down-conversation mixer is shown at Fig. 6. Differential IF outputs are converted to single-ended operation with an external balun circuit (L1, L2 and C1) and DC blocking capacitor C2. The increase of the bias current of Q1 results in the increase of not only the linearity but also noise in this single balanced mixer topology.

The bias current of Q1 was determined to produce high IIP3 (> 0 dBm) with good input matching (> 15 dB). The inductive degeneration using down-bond inductors improves input matching with only a small degradation in mixer noise. R1 and R2 in Fig. 6 were also used to increase the linearity at the cost of degradation of conversion gain.

The noise and input matching was optimized with transistor sizing and on-chip components. The size of switching transistors (Q2, Q3) was traded-off between noise and buffer loading. As for sources of noise, the base resistance of the RF input stage (Q1) is one of the dominant factors; the RF input stage was optimized similar to that of an LNA design. The inductive degeneration using down-bond inductors improves input matching with only a small degradation in mixer noise.
Simulation Results:

The proposed up-conversion mixer is designed by TSMC 0.18-μm CMOS technology and simulated by using Advanced Design System (ADS2010). The total bias current consumed by the proposed mixer is 3-mA with supply voltage of 1.8-V.

The input signal at 5.35GHz is down converted to 350 MHz through a 5 GHz Self LO signal. The conversion gain of the mixer was measured at various RF_Power and the results are shown in Fig. 8. Fig. 9 shows IF spectrum.

Table 1 provides the comparison between performance of the proposed mixer and the most recently published works.
Table 1: Performance Compare.

<table>
<thead>
<tr>
<th>Process</th>
<th>Freq (GHz)</th>
<th>Vdd (V)</th>
<th>I (mA)</th>
<th>CG (dB)</th>
<th>NF (dB)</th>
<th>IIP3 (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gook-Ju Ihm, 2004</td>
<td>0.18</td>
<td>5.25</td>
<td>1.8</td>
<td>12</td>
<td>10</td>
<td>14.5</td>
</tr>
<tr>
<td>Yuan-Kai Chu et al., 2003</td>
<td>0.18</td>
<td>5.8</td>
<td>1.8</td>
<td>6</td>
<td>-4.5</td>
<td>14.6</td>
</tr>
<tr>
<td>Xuezhen Wang and Robert Weber, 2004</td>
<td>0.18</td>
<td>5.8</td>
<td>1.5</td>
<td>7.85</td>
<td>10.4</td>
<td>13.6</td>
</tr>
<tr>
<td>M. Tiebout and T. Liebermann, 0.13</td>
<td>2.15</td>
<td>1</td>
<td>40</td>
<td>5.5</td>
<td>14.5</td>
<td>0</td>
</tr>
<tr>
<td>This Work</td>
<td>0.18</td>
<td>5.35</td>
<td>1.8</td>
<td>3</td>
<td>1.93</td>
<td>12.5</td>
</tr>
</tbody>
</table>

Conclusion:
This paper has presented the design and simulation of a CMOS up-conversion Self-oscillating mixer at 5 GHz for wireless applications. Fundamental signal generated by the oscillator subcircuit in the mixing process the proposed mixer achieved IIP3 of 0dBm with conversation gain of 1.93 dB and consumes only 5.4-mW power at 1.8-V supply.

REFERENCES
Yuan-Kai Chu et al., 2003. “5.7 GHz 0.18 /spl mu/m CMOS gain-controlled LNA and mixer for 802.11a WLAN applications”, RFIC Symposium, pp: 221-224.