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Improved Performance and Power Consumption of Modern FPGAs using a Hybrid CNT/Metal Routing Architecture

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Abstract: Replacing the conventional interconnects with newer material is an effective solution for the serious problems of these interconnects, especially in FPGAs in which more than of 70% of area covered by interconnects. In this paper, using the Carbon Nanotube (CNT) interconnects in FPGAs is explored and a CNT/Metal hybrid routing architecture for large FPGAs is proposed. In the presented architecture, both CNT and metal wires are utilized such that global wires are routed by CNT and local nets are constructed by metal wires. Our experimental results show that this architecture improves critical delay, total wirelength, and total power consumption by 10.87%, 1.28%, and 4.60%, respectively of attempted benchmarks.

Key words: *FPGA, Interconnects, Carbon nanotubes.*

Introduction

In recent years, speed and costs of large VLSI systems getting better dramatically but performance of interconnects getting worse. Replacing the aluminum wires with copper improves characteristics of interconnects but it is not sufficient and using the new technologies such as three-dimensional stacking, optical wires, RF interconnects and Carbon nano-tube interconnects can alleviate the interconnect problems. Carbon nanotube devices can be used as transistors as well as interconnects. Carbon nanotube interconnects have considerable features (vs. metal wires) such as lower resistance and higher durability against electro-migration.

FPGAs are ultra-large circuits that are widely used in various applications, especially for embedded and reconfigurable systems in recent years. Modern FPGAs have a matrix-based regular structure with large number of wires and more that 90% of area and about 60%-70% of delay is related to routing resources (Ma, Y. and M. Lin, 2007). However, they suffer from large overheads (area, delay, and power) because of their programmable interconnect resources, especially for global wires. The negative impact of interconnects on performance of FPGAs is more annoying than ASICs because of two aspects:

- The complexity growth of modern FPGAs is normally more than ASICs [100]. Therefore, more global wires are existed in FPGAs and consequently, restrictive effects of long wires are more considerable in FPGAs.
- Routing resources in FPGAs are more limited than ASICs because FPGA routing is only viable using pre-fabricated channels and switches. Therefore, many of wires may be detoured; consequently, routing congestion, routability and signal integrity problems in FPGAs will be very crucial.

In this situation, improving the interconnect features of FPGAs are very important. On the other hand, FPGAs have large potentials for using the CNT interconnects because FPGAs have regular structure that facilitates the efficiently using the ballistic feature of CNT interconnects for improving the performance of global wires. On the other hand, routing resource limitation in FPGAs causes to detour many of wires. Therefore, number of long wires will be considerable.

Recent FPGAs have various-length wire segments to make a good trade-off between performance and routability. In this structure, short segments have small area and routing congestion for local connections and long wire segments that spans 1, 2, or more switch boxes minimizes the propagation delay for longer connections (Lemieux, G. and S.D. Brown, 1993). The main drawback of using the CNT interconnects inclined with MOS devices in FPGAs is that the contact resistance between CNT and metal interconnects is considerable. On the other hand, ballistic feature of CNT interconnects cause to decrease the delay of long wires dramatically. Therefore, they should be used for enough-long wires to be efficient. Therefore, a reasonable FPGA architecture in which long metal interconnects use CNTIs and local connection employs metals wires with proper ratio of these types of interconnects can make a considerable performance.

Authors of (Eachempati, S., 2007) investigate the effect of statistical variations in interconnect properties and the results show that SWCNT interconnect can provide higher performance over traditional technologies. They show that SWCNT bundle have lower resistance and higher performance for below 45nm technology. In (Eachempati, S., 2007), SWCNT bundles are used in the FPGA interconnects and compare their performance to copper interconnect in future technologies. They explore several aspects of their routing architecture including the segmentation distribution. The results show that FPGAs utilizing SWCNT bundle interconnect can achieve a 19% improvement in average area delay product over the copper interconnect in 22 nm. Authors of

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(Eachempati, S., 2009) consider the performance of routing architectures in FPGAs that use SWCNT bundles as interconnect in next technologies. They explore several prospects of the FPGA routing architecture base on wire length segmentation distribution and also consider the effect of statistical variations in interconnect properties that result in successive placement and routing of benchmarks. In (Hashempour, H., F. Lombardi, 2007), CNTFETs are used as promising devices for implementing high performance circuits in nano-scale. Authors consider the reliability of the CNTFETs in presence of some faults as encountered in MOS devices. For CNTFET-based circuits, these defects are analyzed using a traditional stuck-at fault model. Authors of (Patil, N., 2007) present a technique for designing CNFET-based arbitrary logic functions that are guaranteed to be correct even in the presence of a large number of misaligned CNTs. The energy, delay and area costs associated with such a design technique are significantly lower than traditional fault-tolerance techniques. In (Dong, C., 2009), a new CNT-based FPGA architecture is proposed (called FPCNA) that define novel CNT and nano-switch based components and characterize these components considering nano-specific process variations, including the variation caused by the random mixture of metallic and semiconducting CNTs. In mentioned contributions, some technical aspects of using the CNTIs in FPGAs are evaluated but none of them do not proposed a usable routing architecture and routing algorithm for modern FPGAs. In this paper, we analyzed many of FPGA circuits and then, a hybrid CNT/Metal routing architecture is proposed based on statistical routing information.

In this paper, we evaluated the performance and reliability of FPGAs using CNTIs and then a new FPGA routing architecture is proposed to utilize the benefits of CNTIs. We also compared conventional FPGAs and CNTI-based FPGAs to show improvements of the proposed FPGA architecture.

The rest of the paper is as follows. In the Section 2, we provide a brief background on carbon nanotubes and introduce all types of metal interconnects. Section 3 describes conventional FPGAs. In Section 4, we describe our proposed architecture that how we implement our architecture base CNT interconnects to achieve the best results. Section 5 shows the experimental results and finally, Section 6 concludes the paper.

2 Metal wires vs. Carbon Nanotube Interconnects:

Nowadays, metal interconnects are considered as one of the biggest challenges that designers encounter because of their resistivity, power dissipation, crosstalk noise and electro-migration (Naeemi, A., 2007). Replacing the aluminum with copper result in lower resistance and better electro-migration but it cannot resolve the wire problems because copper wires are going through the similar problems due to the increasing resistivity and wire delay is becoming serious problem. A Carbon Nano-tube is a sheet of graphite called Graphene rolled up into a seamless cylinder with a diameter of a nanometer (Raychowdhury, A., K. Roy, 2004). They have the potential of being used as both transistors and interconnect. Depending on their chirality they can be metallic or semiconductor. In SWCNTs the cylindrical structure consists of a single layer of Graphene. MWCNTs consist of multiple concentric cylinders or the Graphene sheet is simply rolled in around itself. CNTs have unique properties that distinct them from others like their extremely physical and electrical characteristic and also have high density, current, thermal conductivity, less vulnerability to electro migration and their especially mechanical property (Raychowdhury, A., K. Roy, 2004; Banerjee, K., N. Srivastava, 2006; Cassell, A.M., J. Li, 2007; Banerjee, K., N. Srivastava, 2005; Naeemi, A., J.D. Meindl, 2007). CNTIs can be utilized in combination with metals in FPGA and ASIC design methodologies. Using the CNTIs for short lengths is suitable because can growth them easier and faster but the main concern of them is their high contact resistance.

Generally, we divide all kind of interconnects into four groups: short (local), intermediate, long and very long (global) wires. Short interconnects are routed in the lowest level of metal (metal1 or even poly silicon) (Naeemi, A., J.D. Meindl, 2007). For shorter wires, capacitance has a larger impact on performance rather than their resistance (Aimadeddine, M., *et al*., 2007). Reducing the effective dielectric constant can allow designers to achieve the same performance while reducing the demands placed on the metal wires. They are very sensitive to contact resistance because of their small lengths (Naeemi, A., J.D. Meindl, 2007). Intermediate wires are longer than local wires and they route in metal levels above the local wires. They have smaller resistance and less sensitive to contact resistance. Sometimes may need using repeaters to improve their delay. In this type of wires, replacing the metal wires with CNT bundles may increase their conductivity and decrease their latency. Long and global wires are longer than others. They normally are data busses between macro-cells (Naeemi, A., J.D. Meindl, 2007). Therefore, CNT bundles can increase flexibility and conductivity of these wires. Resistance is more important for long wires and reduction in their resistance can help them to have higher speed and lowers the delay.

Recent research shows that more than 70% of delay in FPGAs is related to interconnect resources. On the other hand, routing resources in FPGA are very restricted by the number of available channels and switch boxes. Moreover, FPGAs have regular structure with various length wire segments that have considerable resistance and delay. In this situation, FPGAs can utilize the benefits of CNTs efficiently.

3 Statistical Analysis of FPGA Interconnects:

As mentioned before, CNT interconnects can be used for enough-long wires to be efficient. In this section, number and ratio of various types of interconnects (short, intermediate and long) in modern FPGAs are analyzed statistically on standard benchmarks. Results of this analysis are used as important information for proposing the suitable architecture for CNTI-based FPGA.

In compare of ASICs, they have some advantages and disadvantages, for example they support Moore's low but they consume 10x much more dynamic power, 2 to 3.5x more area and 3 to 4x slower than ASICs (Kuon, I., 2008). Generally, the FPGA routing is utilizes the wire segments and switch-boxes. Modern FPGA architectures have various length wire segments enabling the router to choose suitable wire segments for each wire. Long wire segments have considerable resistance and replacing them with CNTIs can improve delay and power consumption of the FPGA considerably. However, FPGA delay and power can be improved by replacing with CNTIs when the number of long wire segment is significant. Our analyses are preformed to provide this information.

We performed a dozen of experiments on FPGA EDA tool showing the distribution of long wires around the FPGAs. Results of these experiments helps us to design an efficient CNTI-based FPGA architecture. We used VPR (Betz, V., J. Rose, 1997) as FPGA EDA tool and larger circuits from MCNC benchmarks are selected as attempted benchmarks. General information of attempted benchmarks is shown in Table 1. In this table, column Dimension represents the number of row and columns in each benchmark and columns #Nets, #Blocks, #Clbs, #Inputs, #Outputs and #Tracks show the number of nets, blocks, clbs, inputs, outputs and tracks, respectively.

Table 1: MCNC Benchmarks.

No	Benchmark	Dimension	#Nets	#Blocks	#Clbs	# Inputs	#Outputs	# Tracks
1	alu4	40 × 40	1536	1544	1522	14	8	451
2	apex2	44 × 44	1916	1919	1878	38	3	540
3	apex4	36 × 36	1271	1290	1262	9	19	518
4	bigkey	54 × 54	1936 + 1 G	2133	1707	229	197	385
5	clma	92 × 92	8445 + 1 G	8527	8383	62	82	1302
6	des	63 × 63	1847	2092	1591	256	245	576
7	diffeq	39 × 39	1561 + 1 G	1600	1497	64	39	360
8	dsip	54 × 54	1599 + 1 G	1796	1370	229	197	385
9	e64-4lut	17 × 17	309	404	274	65	65	144
10	e64-4x4lut	9 × 9	290	200	70	65	65	190
11	elliptic	61 × 61	3735 + 1 G	3849	3604	131	114	744
12	ex5p	33 × 33	1072	1135	1064	8	63	510
13	ex1010	68 × 68	4608	4618	4598	10	10	897
14	frisc	60 × 60	3576 + 1 G	3692	3556	20	116	915
15	misex3	38 × 38	1411	1425	1397	14	14	468
16	pdc	68 × 68	4591	4631	4575	16	40	1311
17	s298	44 × 44	1935 + 1 G	1941	1931	4	6	450
18	s38417	81 × 81	6435 + 1 G	6541	6406	29	106	738
19	s38584	81 × 81	6485 + 1 G	6789	6447	38	304	738
20	seq	42 × 42	1791	1826	1750	41	35	559
21	spla	61 × 61	3706	3752	3690	16	46	992
22	tseng	33 × 33	1099 + 1 G	1221	1047	52	122	272

G=Global Net

We used 32nm technology node parameters in architecture file VPR. Moreover, our main assumptions about the FPGA are as the following:

- Length of a wire segment in this paper is the number of CLBs spanned by the segment.
- Distance between two adjacent CLBs (FPGA channel length) is assumed as $20\mu m$.
- Length of the short (local) interconnects is less than $20\mu m$.
- Intermediate interconnects are those nets whose length are larger than $20\ \mu m$ and less than $100\mu m$.
- Length of long interconnects base on (Naeemi, A. and J.D. Meindl, 2006) is between $100\mu m$ and $400\mu m$.
- Very long (global) interconnects' length is larger than $400\mu m$.

CNT interconnects are inherently suitable for long nets. Therefore, our focus in this paper is on long interconnects. We changed the VPR (Betz, V., J. Rose, 1997) to calculate the length of all type of interconnects after placement and routing. Then, investigate percentage of long interconnects rather than others. This comparison is shown in figure 1 and averages of these distributions are shown in table 2.

Table 1: Average of different length interconnects.

Distribution	>L(%)	>L/2(%)	>L/3(%)	>L/4(%)	>L/5(%)	>L/6(%)	=1(%)
average	0.024	0.08	0.11	0.14	0.15	0.17	0.24

In figure 2 and table 2, all columns are base wire length segmentation distribution of each benchmark, column ">L" represent the interconnects that their length is equal to dimension of FPGAs (Longline) and ">L/2", ">L/3", ">L/4", ">L/5" and ">L/6" represent the 1/2,1/3,1/4,1/5 and 1/6 of their real length and column "=1" represent single length.

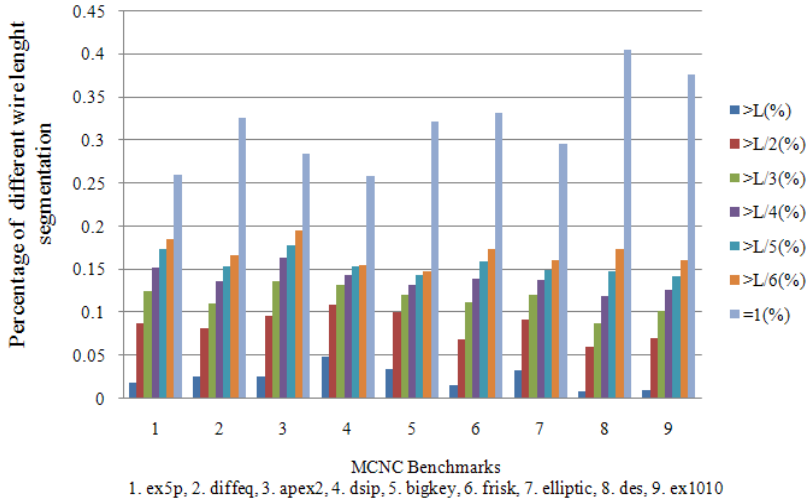

Fig. 1: Results for different wire length segmentation distribution in MCNC benchmarks

Base of this division can achieve the exact ratio of interconnects as shown in table 3. so, for example, length =1 means a segment that spans 1 CLB and length = 6 means a segment that spans 6 CLBs and just cross from the first and last SB and skip from others, as shown in figure 2.

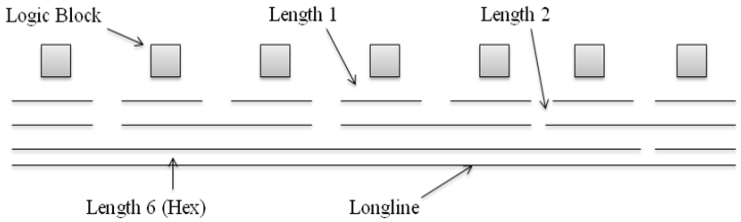

Fig. 2: Example wire length segmentation.

To attention to figure 2, can compare ratio of different interconnects to each other, as shown in figure 4 and average of all type of interconnects is shown in table 3, exactly on average. In table 3, percentage of local, intermediate and long interconnects are represented. As shown in this table, the number of long wires in an FPGA is not very small.

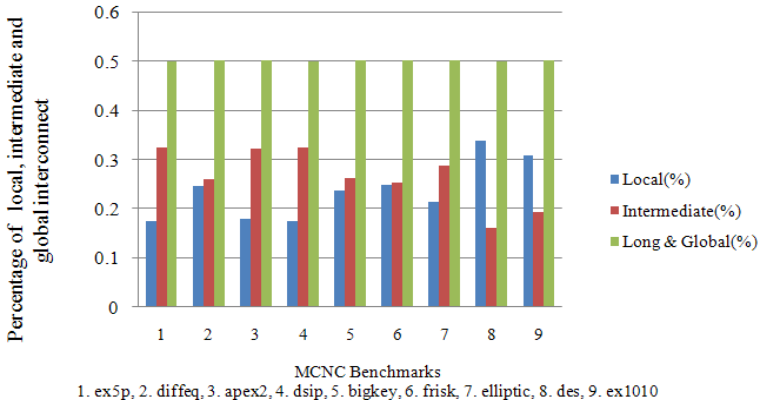

Fig. 3: Results that achieve from figure 2 to calculate all type of interconnects exactly in each benchmark.

Results that achieve from Table 2 to calculate all type of interconnects exactly

Base of figure 3, calculate the average of local, intermediate and long interconnects in MCNC benchmarks as shown in table 3.

Table 2: Percentage of all kind of interconnects on average.

Benchmark	Local(%)	Intermediate(%)	Long & Global(%)
Average	0.234	0.265	0.5

As mentioned before, a channel with Length =1 connects two adjacent switch boxes and we assumed real length of a local wire with length=1 as $20\mu m$. To divide the wires into local, intermediate and global, length of the wires are calculated. For example, L/2 and L are global interconnects in benchmark *apex2* because their dimension (L=44 or $44 \times 20\mu m = 880\mu m$ and L/2 means$22 \times 20\mu m = 440\mu m$) and L/3, and L/4 are long interconnects (e.g. $L/3 \cong 15$ or$15 \times 20\mu m = 300\ \mu m$). Results that shown in *Long & global (%)* column represent that half of wires that use in each benchmark are long and global. As shown above 0.23 % of interconnects are local, $\cong 0.26\%$ of them are intermediate, 0.5% of them are long and global. As can be seen in Table 3, considerable portion of FPGA wires are global. Therefore, using the CNT interconnects can be efficient in these circuits. In the next section, a CNT/metal hybrid architecture is described to uses the benefits of metal and CNT wires. Also ratio of long interconnects to others shown on table 4.

Table 3: Ratio of long interconnects to others

Benchmark	Long/Local(%)	Long/Inter(%)
ex5p	2.851429	1.535385
Diffeq	2.040816	1.930502
apex2	2.793296	1.557632
Dsip	2.867816	1.535385
Bigkey	2.118644	1.901141
Frisk	2.017756	1.984127
Elliptic	2.347418	1.74216
Des	1.471976	3.099379
ex1010	1.628664	2.590674
average	2.137535	1.886265

In table 4, base of last results that represent in table 2 and table 3, investigate the ratio of long interconnects to local and intermediate, because base of our assumption wires with at least $100\ \mu m$ have capability to replace with CNTI. As shown before, these wires are half of these wires. So, replacing them have superior benefit to have higher performance. Results show that: ratio of long to local is about $2.1x$ and long to intermediate is $1.8x$. so long interconnects are more than others and in locals we have contact resistivity that is a limitation to use them for CNTIs.

4 Proposed Architecture:

In this section, we present a new architecture which utilizes both CNT and metal wires in large FPGAs. As mentioned before, the wires whose lengths are larger than $100\ \mu m$ can be replaced with CNTI. In other means, short channels are made with metal and long channels are implemented using CNTI interconnects. As mentioned before, length of a channel is $20\mu m$. Therefore, minimum length for CNT interconnect should be $(5 \times 20\mu m = 100\ \mu m)$.

In the proposed model, basic design of the FPGA is remained unchanged but some auxiliary channels are added to the FPGA. The length of auxiliary channels is at least 5 CLBs. It is assumed that these wire segments are build with CNTIs. This structure is shown in Figures 4 and figure 5.

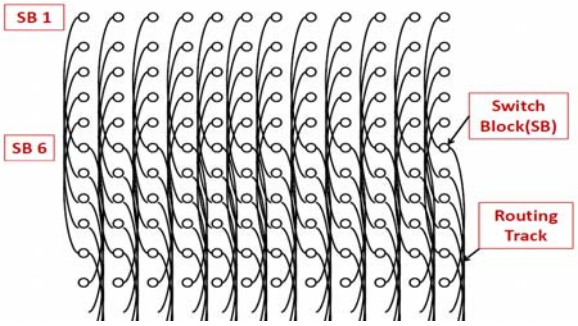

Fig. 4: Results from vertical routing (L= 5 CLB).

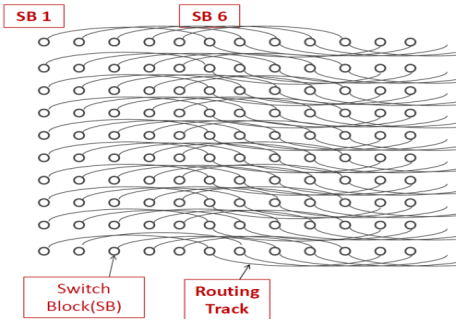

Fig. 5: Results from horizontal routing (L= 5 CLB).

As can be seen in Figures 4 and 5, each switch box is connected to one vertical and horizontal CNTI channel. This structure simplifies all vertical, horizontal and diagonal connections. An example of a diagonal connection on the proposed architecture is shown in Figure 6.

The important concern in this model is the length of interconnects in the architecture that is enough to use CNT interconnects.

5 Experimental results:

As mentioned before, we used VPR FPGA tool for evaluating the contribution. Therefore, we changed the routing model (Betz, V., 1999) of VPR to support auxiliary CNTI channels to implement the proposed architecture. This graph is shown in Figure 6.

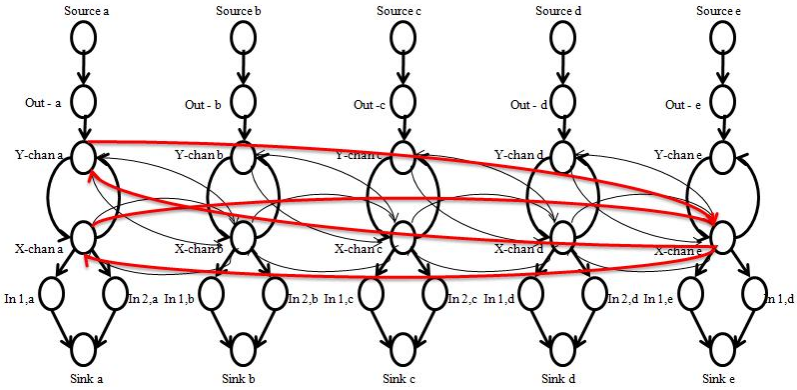

Fig. 6: Routing graph that results from CNTIPGA.

That can write:

$y_{chan_a} = x_{chan_b}$ $x_{chan_b} = y_{chan_a}$ $x_{chan_a} = x_{chan_b}$ $x_{chan_b} = x_{chan_a}$	$y_{chan_b} = x_{chan_c}$ $x_{chan_c} = y_{chan_b}$ $x_{chan_b} = x_{chan_c}$ $x_{chan_c} = x_{chan_b}$	$y_{chan_c} = x_{chan_d}$ $x_{chan_d} = y_{chan_c}$ $x_{chan_c} = x_{chan_d}$ $x_{chan_d} = x_{chan_c}$	$y_{chan_d} = x_{chan_e}$ $x_{chan_e} = y_{chan_d}$ $x_{chan_d} = x_{chan_e}$ $x_{chan_e} = x_{chan_d}$	$y_{chan_a} = x_{chan_e}$ $x_{chan_e} = y\_chan\_a$ $x_{chan_a} = x_{chan_e}$ $x_{chan_e} = x_{chan_a}$

We developed our routing model in VPR FPGA tool. Our algorithm is implemented on an Intel Dual Core processor with 2GB of main memory. MCNC circuits are selected as attempted benchmarks with different wire length segmentation distribution as shown in Table 5.

Table 5: Different wire length segmentation distribution.

Segmentation Distribution	1	2	6	Longline
1st dataset	0.23	0.27	0.38	0.12
2nd dataset	0.1	0.2	0.5	0.2
3rd dataset	0.1	0.3	0.4	0.2
4th dataset	0.3	0.3	0.2	0.2
5th dataset (Lemieux, G. and S.D. Brown, 1993)	0.08	0.2	0.6	0.12

According to table 5, we segmented wires into 4 groups (base on our assumption): 1 as local wires (1 × 20µm= 20 µm), 2 as intermediate wires (2 × 20µm= 40 µm), 6 as long (6 × 20µm= 120 µm) and longline that depend to FPGA size is variable but because we choose the largest of MCNC benchmarks, longline is as global wires.

First dataset is our proposed wire length segment that base on exact ratio of all type of interconnects that calculate in prior section. VPR (Betz, V., J. Rose, 1997) and PowerModel (Poon, K., 2005) tools are used for all of the structures shown in Table 5 to calculate power, speed and area base 6 key parameters.

5.1 Comparison of CUI and CNTI in First Wire Length Segmentation Distribution:

In this section we compare 6 main factors that utilized in FPGAs to have higher performance and more reliability. We compare 5 different wire length segmentation distribution that first of it , is base of our results in section 3 (exact ratio of long wires to others) and others are base on random wire length distribution, we use these distributions to 2 reasons:

1. If we use hybrid (CNT/metal) architecture for FPGA, we certainly have improvement in area, delay and power (CNTIPGA is useful to improve performance of ultra-large FPGAs).
2. but, if we use exact ratio of wire length segmentation distribution, we achieve the highest and best improvement than others.

5.1.1 Critical, Net and Logic Delay:

In this sub-section, improvement of the CNT/metal hybrid architecture in term of the performance is reported. Table 6 shows the critical path, net delay and logic delay improvement of the proposed architecture vs. conventional FPGA architecture is addressed.

Table 6: Experimental results for delays from CNTIPGA

	CU			CNT			Improvement (%)		
Benchmark	Logic-D	Net-D	Crit-D	Logic-D	Net-D	Crit-D	L-D	N-D	C-D
apex2	4.05E-009	7.23E-008	7.64E-008	4.60E-009	7.55E-008	8.01E-008	-13.485058	-4.42021181	-4.90083773
bigkey	2.42E-009	4.96E-008	5.20E-008	2.42E-009	5.07E-008	5.31E-008	0	-2.28399408	-2.17787380
clma	6.24E-009	1.73E-007	1.79E-007	6.24E-009	1.37E-007	1.43E-007	-0.00048100	20.8599527	20.1339285
des	3.50E-009	6.94E-008	7.29E-008	2.41E-009	5.91E-008	6.15E-008	31.1732800	14.9020952	15.6837736
diffeq	8.42E-009	4.53E-008	5.37E-008	1.87E-009	5.58E-008	5.76E-008	77.8054599	-23.2455723	-7.39224800
dsip	2.42E-009	5.42E-008	5.66E-008	2.42E-009	4.02E-008	4.26E-008	0	25.8096169	24.7089984
elliptic	1.87E-009	1.05E-007	1.07E-007	4.60E-009	6.88E-008	7.34E-008	-146.067415	34.4319330	31.2717445
ex5p	3.50E-009	8.01E-008	8.36E-008	4.05E-009	5.84E-008	6.25E-008	-15.5863100	27.0429541	25.2567651
ex1010	5.14E-009	1.59E-007	1.65E-007	5.14E-009	1.25E-007	1.30E-007	-0.00077806	21.6954852	21.0175713
frisk	1.17E-008	9.79E-008	1.10E-007	5.69E-009	1.22E-007	1.27E-007	51.3464991	-24.3694630	-16.2913097
pdc	5.14E-009	1.92E-007	1.97E-007	5.14E-009	1.43E-007	1.48E-007	-0.00058354	25.5419661	24.8744357
s38417	2.42E-009	8.01E-008	8.25E-008	2.41E-009	6.67E-008	6.91E-008	0.16521739	16.7112062	16.2268345
seq	3.50E-009	7.28E-008	7.63E-008	4.05E-009	5.95E-008	6.36E-008	-15.5863100	18.2503188	16.6976700
spla	5.14E-009	1.25E-007	1.31E-007	3.50E-009	1.44E-007	1.47E-007	31.8620271	-14.6662093	-12.8333231
average	4.67E-009	9.83E-008	1.03E-007	3.89E-009	8.60E-008	8.99E-008	0.11611050	9.73286270	10.8768664

As shown in table 6, with CNTIPGA distribution, average of critical delay for copper is $1.03 \times 10^{-7}\ ps$ and for CNT is $8.99 \times 10^{-8}\ ps$ that have improvement about 10.88%. Figures 7, 8 and 9 are shown difference in average of Net, Logic and Critical delay between copper and CNT, that in all of them have considerable improve.

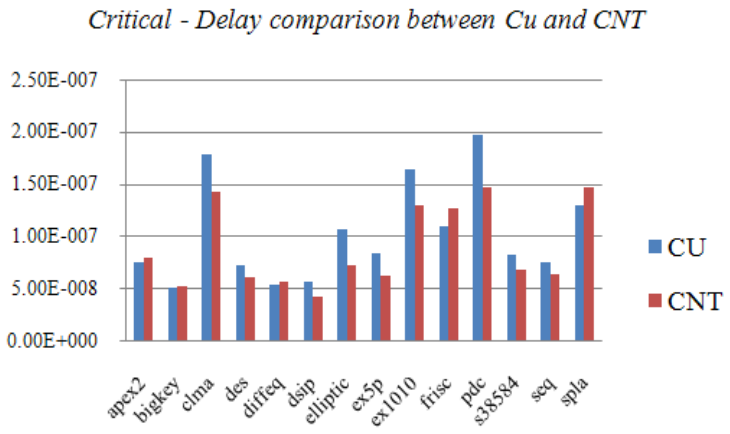

Fig. 7: Average of critical delay comparison between CUI and CNTI.

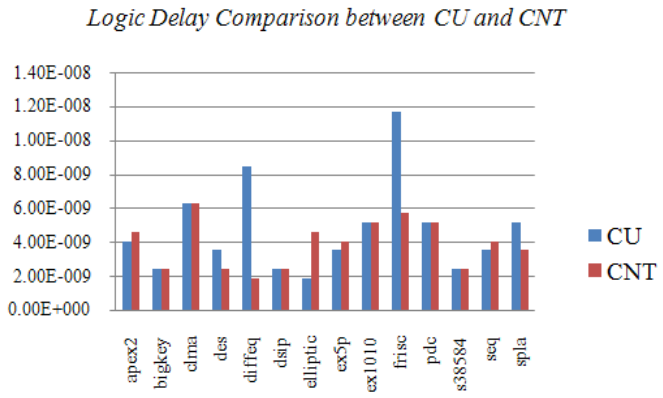

Fig. 8: Average of logic delay comparison between CUI and CNTI.

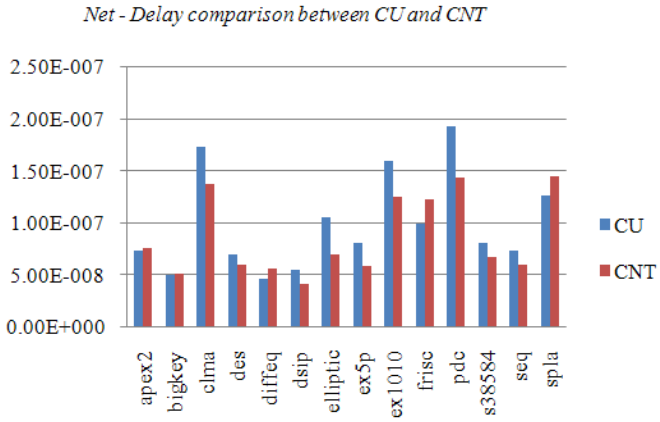

Fig. 9: Average of net delay comparison between CUI and CNTI.

Table 6 shows the net delay, logic delay and critical path improvement of the proposed architecture vs. conventional FPGA architecture is addressed. As can be seen in Table 6, using the proposed architecture decreases the critical delay by 10.87% on average, net delay 9.7% and logic delay 0.12%, respectively. Moreover, it can be seen that the results are better for larger circuits where more global wires can be found.

5.1.2 Total Wire Length:

In this section, improvement of FPGA area and total wirelength are shown. Table 7 represents the experimental results in term of total wire length of the FPGA improvement of the proposed architecture in compare with the conventional FPGA routing scheme. As shown in Table 7, total wire length is improved by 1.28% and 0.21% on average, respectively.

Table 4: TWL comparison in CNTIPGA.

Benchmark	CNT	CU	Improvement (%)
apex2	17089	17780	3.886389
bigkey	13718	13666	-0.38051
clma	77976	79897	2.404346
des	15254	16579	7.992038
diffeq	9715	9346	-3.94821
dsip	12432	12154	-2.28731
elliptic	26914	27728	2.935661
ex5p	9900	10151	2.472663
ex1010	39163	38047	-2.93321
frisk	31815	32229	1.284557
pdc	53069	52635	-0.82455
s38417	34864	35891	2.861442
seq	15979	16127	0.917716
spla	39168	40621	3.576968
Average	28361.14	28775.07	1.28271326

As shown in table 7, TWL comparison between copper and CNT and results shown that with CNTIPGA, total wire length for copper is 28775.071 μm and for CNT is 28361.14 μm that have 1.29% improvement.

5.1.3 Minimum Channel Width (Wmin):

In this sub-section compare minimum channel width (W_{min}) between copper and CNT as shown in table 8.

Table 8: Minimum channel width difference between CUI and CNTI.

Benchmark	CNT	CU	Improvement (%)
apex2	27	27	0
bigkey	18	21	14.2857143
clma	34	32	-6.25
des	25	25	0
diffeq	18	18	0
dsip	18	21	14.2857143
elliptic	26	25	-4
ex5p	32	26	-23.076923
ex1010	28	27	-3.7037037
frisc	27	29	6.89655172
pdc	37	37	0
s38584	23	24	4.16666667
seq	26	26	0
spla	35	39	10.2564103
average	26.7142857	26.9285714	0.21428571

Table 8 represents the experimental results in term of minimum channel width of the FPGA and as shown, have 0.21% improvemnet in minimum channel width that when W_{min} decrease cause decrease in area

5.1.4 Power Dissipation:

As mentioned before, CNT interconnects have lower resistance and parasitic capacitance. Therefore they made lower power consumption, especially for long wires. In this sub-section, improvement of CNT-based architecture is compared with the conventional FPGAs. Figure 10 show the difference in power dissipation between hybrid architecture and conventional FPGA and figure 11 represent Total power improvement and overhead of CNTI vs. regular FPGA in each benchmark. These results are extracted from PowerModel tool (Clarke, P., E.E. Times, 2009).

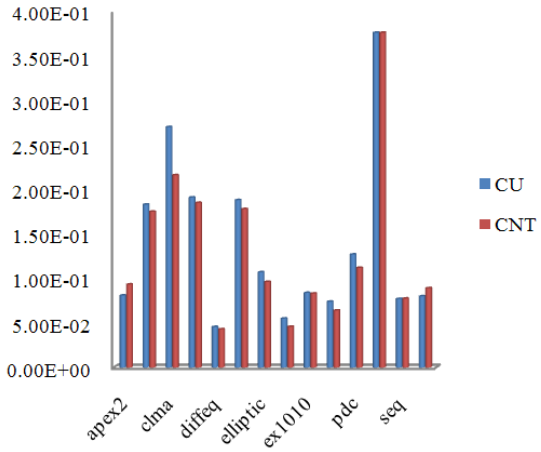

Fig. 10: Difference in power dissipation between hybrid architecture and conventional FPGA.

As shown in figure 10 and 11 total power dissipation have significant reduction by using proposed architecture especially in larger benchmarks that have more longer interconnects. In table 9 average of total power consumption in benchmarks when just use CUIs and when use hybrid interconnects are shown and represent that with proposed architecture can achieve 4.6% improvement on total power consumption on average, respectively.

5.1.4 Leakage Power Consumption:

In this section, calculate leakage power dissipation in copper and CNT and compare them, as shown in table 10.

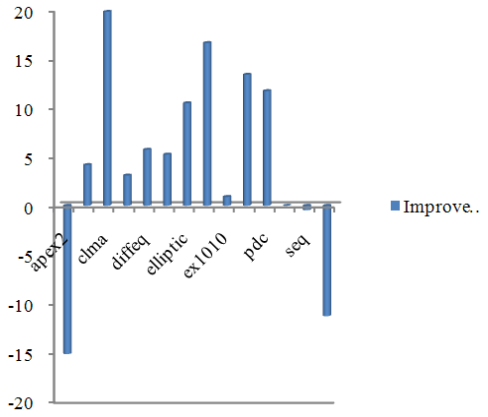

Fig. 11: Final improvement and ovehead amount of each benchmark when use proposed architecture (%).

Table 9: Power dissipation between CUI and CNTI

Benchmark	CU	CNT	Improvement (%)
average	1.38E-001	1.31E-001	4.5960497

Table 10: Comparison between leakage power consumption in CNTIPGA.

Benchmark	CU	CNT	Improve(%)
apex2	1.29E-002	1.23E-002	4.702399
bigkey	1.33E-002	1.31E-002	1.6994996
clma	5.34E-002	5.12E-002	4.020941
des	1.59E-002	1.49E-002	6.3149868
diffeq	8.11E-003	7.93E-003	2.1537729
dsip	1.33E-002	1.18E-002	11.716879
elliptic	1.80E-002	1.74E-002	3.3085259
ex5p	7.65E-003	7.57E-003	1.0093509
ex1010	3.40E-002	3.27E-002	3.8417328
frisc	2.12E-002	2.13E-002	-0.4845794
Pdc	3.72E-002	3.51E-002	5.781195
s38417	4.33E-002	4.79E-002	-10.564337
seq	1.26E-002	1.20E-002	4.7346394
spla	2.94E-002	2.86E-002	2.5502063
average	2.29E-002	2.24E-002	2.9132295

As shown in table 10, leakage power consumption for regular FPGA is $2.29 \times 10^{-2} W$ and for hybrid FPGA is $2.24 \times 10^{-2} W$ that leakage power is improved by 2.9%.

5.1.5 Energy Consumption:

In this sub-section, improvement of CNT-based architecture is compared with the conventional FPGAs. Table 11 represents the Total energy consumption improvement of CNTI vs. regular FPGA.

Table 11: Energy consumption in CUI and CNTI .

Benchmark	CU	CNT	Improve(%)
apex2	9.70E-009	8.48E-009	12.542714
bigkey	1.07E-008	9.44E-009	11.956453
clma	5.51E-008	5.29E-008	3.9894283
des	1.34E-008	1.23E-008	7.8457337
diffeq	6.15E-009	5.58E-009	9.2893804
dsip	8.78E-009	8.37E-009	4.6901886
elliptic	1.85E-008	1.63E-008	12.105283
ex5p	4.46E-009	4.18E-009	6.3444793
ex1010	1.55E-008	1.43E-008	7.415797
frisk	1.80E-008	1.53E-008	14.968312
pdc	2.01E-008	1.95E-008	2.8993871
s38417	4.35E-008	3.87E-008	11.19217
seq	9.34E-009	8.42E-009	9.8885621
spla	1.52E-008	1.35E-008	11.21057
average	1.77E-008	1.62E-008	9.0241757

As shown in table 11, energy consume for copper interconnects is $1.77 \times 10^{-8}\,J$ and for CNT is $1.62 \times 10^{-8}\,J$ that decreases by 9.02% after CNTIPGA.

Generally total power, leakage power and energy consumption have direct impact to reduce dynamic power overhead in FPGAs, TWL and W_{min} have high effect to reduce area and decrease in critical delay can help to have higher performance in FPGAs.

5.2 Comparison of Total Results in all Architectures:

AS mentioned before, we examine various wire length segmentation distribution in CNTIPGA that described in Table 4. Figure 12 represents the performance (critical delay) improvements that achieve in all datasets. Figure 13 represents the area consumption (TWL and W_{min}) improvements and Figure 14 represents the reduction in dynamic power that achieve from total power, leakage power and energy consumption in all datasets Our analyses show that CNTIPGA is an effective solution to solve FPGAs problems with each wire length distribution but achieves the best results when the first dataset that is base on exact ratio of interconnects is used.

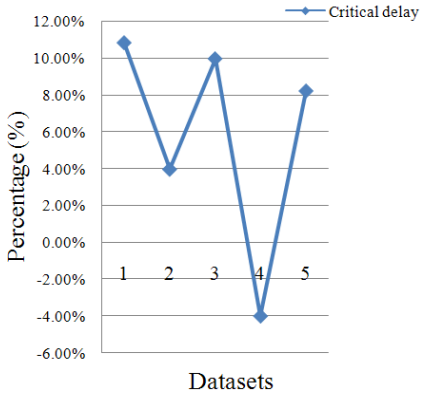

Fig. 12: Critical delay comparison in all datasets. First dataset that utilized exact ratio of interconnects achieve higher performance than others.

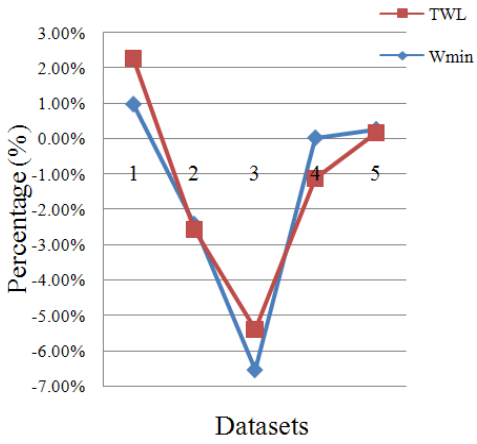

Fig. 13: Total wire length and minimum channel length comparison in all datasets that these improvements have impact in area.

6 Conclusion:

In this paper, we proposed a hybrid CNT and metal routing architecture for FPGAs and investigated the characteristics of the proposed architecture in comparison of metal-based FPGAs. Our experimental results show that critical delay, total wirelength, channel width and total power consumption are improved by 10.87%, 1.28%, 0.99%, and 4.60% on average for attempted benchmarks. Our analyses represents that the results are better for larger FPGAs that have more global wires and 50% wires in FPGAs are long and global. Our outgoing research is focused on exploring the benefit of CNT interconnects in 3D FPGAs.

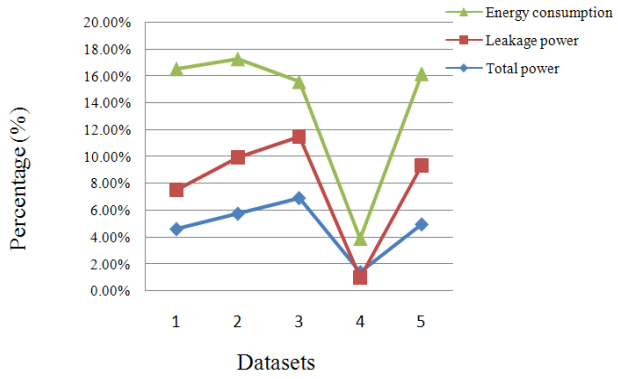

Fig. 14: Total power, leakage power and energy consumption that achieve in all datasets that these improvements have high effect on decrease in dynamic power.

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