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# A New Test Scheme for Process Variation-Induced Faults in Resistive RAMs

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**ABSTRACT**

Resistive random access memory (RRAM) is vying to be one of the main universal memories for computing systems. Nonetheless, due to infancy knowledge and technology to fabrication RRAM, this emerging memory technology is expected to be impacted by processvariation-induced faults. Due to their varying behavior, processvariation-inducedfaults are problematic to be detected using existing test approach that is solely based on the March test concept. This manuscript presents a new test scheme based on the combination of the Design-for-Testability (DfT) concept with the March test concept to detect such faults. Unlike the conventional DfT that asserts a single, fixed write voltage during testing, the proposed test scheme asserts multiple voltage levels that can be digitally adjusted. Simulation results using Verilog-AMS and HSPICE tools show that the processvariation-induced faults can be detected with minor circuit modification. In addition, as the proposed test approaches are programmable, the proposed test scheme alleviates the redesign phase and in turn accelerates time-to-market.



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## INTRODUCTION

Resistive random access memory (RRAM) is vying to be one of the main universal memories for computing systems. RRAM uses the resistive effect of memristive devices (memristor) to store data permanently even in the absence of the power supply (Yang and Pickett *et al*., 2008), (Karg and Meijer *et al*., 2008). Moreover, memristor can be used as the storage element without requiring access transistors; this enables a crossbar memory cell array structure. Furthermore, the memory cell array can be stacked on the top of the CMOS peripheral circuits creating three-dimensional ICs (Strukov and Likharev *et al*., 2008). With such novel devices and advanced circuit architecture, RRAM offers attractive advantages such as enormous storage capacity, low power consumption, simple fabrication for cell array, etc. (Yang and Pickett *et al*., 2008), (Karg and Meijer *et al*., 2008), (Strukov and Likharev *et al*., 2008).

Because of the above-mentioned potentials and commercialization efforts, the research on such a memory technology is growing. To this end, most of the work published so far focuses mainly on the fabrication techniques and reliability improvement using fault tolerance schemes (Strukov and Likharev *et al*., 2008), (Xu and Dong *et al*., 2011), (Ho and Huang *et al*., 2011), (Strukov and Likharev, 2007), (Haron and Hamdioui, 2009), (Haron and Darsono *et al*., 2012). However, research on defect analysis, testing and design for testability for such devices is still in its infancy stage. A previous work has identified unique faults in RRAM cell array, which require requires new test approaches other than March test patterns alone (Haron and Hamdioui, 2011). Although the proposed test approaches – developed based on Design-for-Testability (DfT) concept – are able to detect the targeted faults (Haron and Hamdioui, 2012), they might not efficient to detect faults with different values (e.g., caused by process variations).

This manuscript presents a new test scheme to detect faulty RRAM cells induced byprocess variation problems. The test scheme is developed by combining the Design-for-Testability (DfT) concept with the march test. Owing to its programmability, this new DfT scheme is able to improve fault coverage further compared to state-of-the-arts and alleviate overkilling of RRAM cells. Instead of using a single, fixed write voltage during testing (Haron and Hamdioui, 2012), the proposed DfT scheme uses multiple voltage levels that can be digitally adjusted. Referred to as Programmable Low Write Voltage (PLWV), this proposed DfT scheme ensures process variation-induced faultshavingopen resistive values can be detected; therefore, achieving a better fault coverage and alleviating overkill.

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The rest of the manuscript is organized as follows. The next section discusses the RRAM model and operations. It is followed by an overview of the published work on the fault analysis and test based on a DfT scheme for RRAM, as well as the limitation of the DfT scheme. Thereafter, the manuscript introduces the PLWV scheme including its concept, design methodology, circuit and SPICE simulation results. The manuscript ends with the conclusion.

***RAM model and operation:***

This section briefly reviews the RRAM functional model and its cell electrical model based on memristors. Then, the RRAM write and read operations will be explained.

Fig. 1 depicts the functional block diagram of the RRAM model proposed in (Haron and Hamdioui, 2012), (Strukov and Snider *et al*., 2008). The memory consists of three main parts: (i) non-CMOS cell array, (ii) CMOS-to-Nano Vias (CNVs), and (iii) CMOS peripheral circuits. The peripheral circuits consist of the functional units that are similar to those used in existing semiconductor memories. A detailed description can be referred to (Hamdioui and Van Der Goor, 2000).

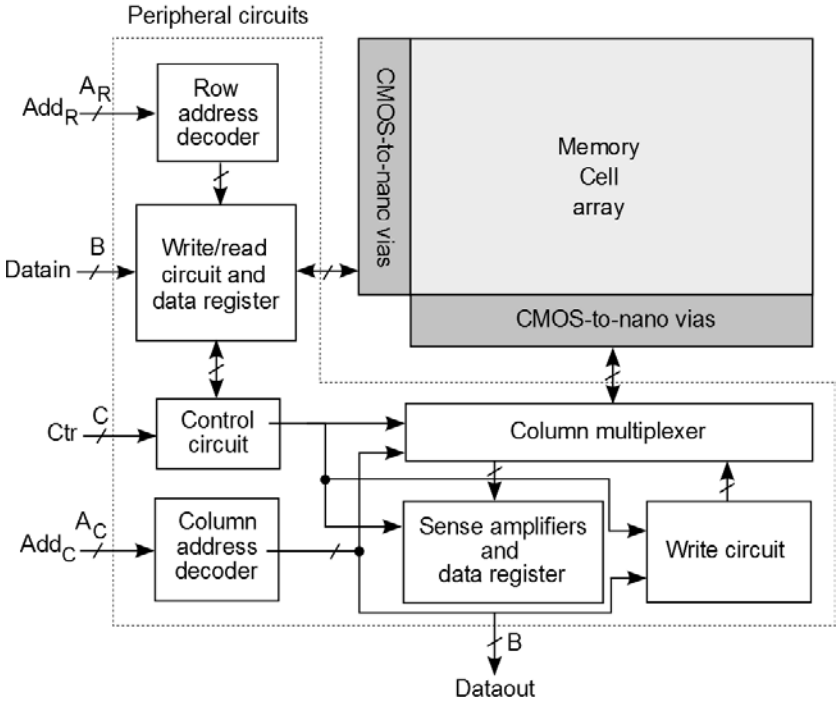


**Fig. 1:** Typical block diagram of RRAM functional model.

RRAM cells are based on memristors, which are two terminal devices that retain their internal resistance even when the supply power is switched off. Figure 2(a) and (b) illustrate the memristor introduced by Hewlett-Packard (HP) researchers and its equivalent electrical model, respectively Strukov and Snider *et al*., 2008).The HP's memristor is fabricated using a thin film of titanium oxide altered with different oxygen atom doping rates, resulting in doped and undoped layers. The doped layer (with thickness w) corresponds to a low memristance$R_{ON}$, while the undoped layer (with thickness $D - w$) corresponds to a high memristance$R_{OFF}$ where$D$ the total thickness of the memristor.

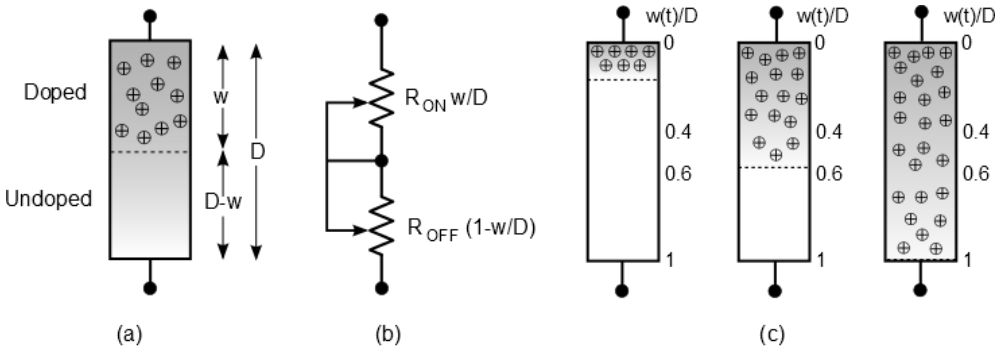


**Fig. 2:** Memristor (a) model (b) equivalent electrical circuit (c) logic 0, undefined,logic 1 definition.

The equivalent electrical circuit of a memristor is modeled as a coupled variable resistor with voltage-current relation as follows (Strukov and Snider *et al*., 2008).

$$v(t) = i(t)\left(R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right) \quad (1)$$

$$\frac{w(t)}{D} = 1 - \sqrt{1 - \frac{2\mu_v \emptyset(t)}{\beta D^2}} \quad (2)$$

Where$\frac{w(t)}{D}$ is the thickness of the doped layer (normalized to the total length of memristor) that changes with time, $\emptyset(t) = \int_0^T V(t)dt$is the injected flux across the memristor for T period, $\mu_v$is an average dopant mobility and $\beta = \frac{R_{OFF}}{R_{ON}}$.

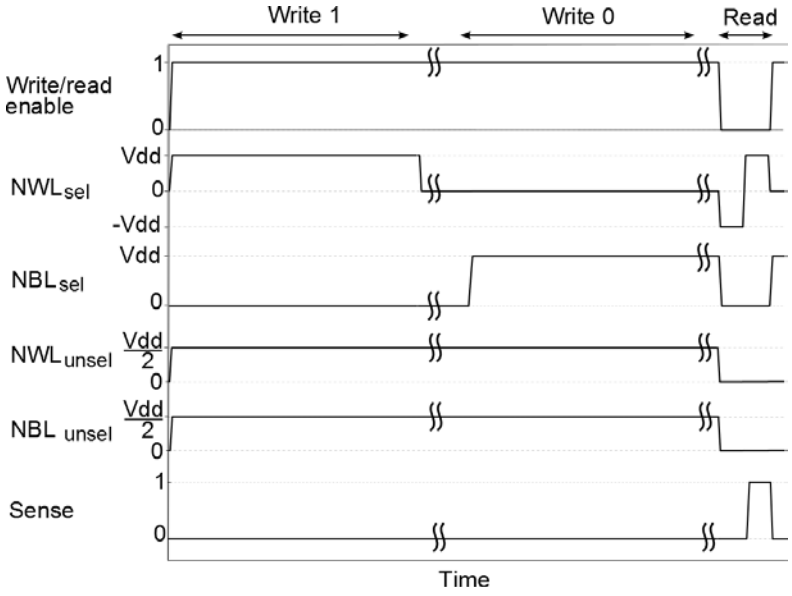


**Fig. 3:** Timing diagram for RRAM write and read operations.

The$\frac{w(t)}{D}$is the metric used to define the logic value hold by a memristor (also referred to as memristor internal state) (Strukov and Snider *et al*., 2008). The value of$\frac{w(t)}{D}$represents the drift of the memristor's dopants and has an inverse correlation compared with its memristance. Because memristors used as RRAM cells are analog devices, yet RRAM operates in binary numbers, the logic state definition as proposed in (Ho and Huang *et al*., 2011) is used. Fig. 2(c) shows that logic 1 is defined for$0.6 \leq \frac{w(t)}{D} \leq 1$ and logic 0 is defined for$0 \leq \frac{w(t)}{D} \leq 0.4$; where $D = 1$. A safety margin$0.4 \leq \frac{w(t)}{D} \leq 0.6$ is set as undefined logic state, which should be avoided for RRAM to operate optimally.

The selected cell is written and read by biasing sufficient voltages across the cell asshown in Fig. 3 (Xu and Dong *et al*., 2011), (Haron and Hamdioui, 2012). The figure shows that logic 1 is written into the selectedcell by biasing$V_{dd}$ from the selected nanowire wordline $NWL_{sel}$ (the positive terminalof the cell) while grounding the selected bitline $NBL_{sel}$ (the negative terminalof the cell). Reversing the biasing voltage polarity will write logic 0. The unselected cells are biased with$\frac{V_{dd}}{2}$, both from their positive and negative terminals.The cells are read by biasing the selected cells are with$-V_{dd}$ in the first half and$+V_{dd}$ in the second half at their positive terminal; at the same time their negativeterminal is connected to the sense amplifier. The unselected cells are left floating.

To ensure that an ideal logic state is written, a write operation requires an ample write time $T_{write}$ . For a given write voltage$V_{write}$ value and $0 \leq D \leq 1$, the required time for an appropriate write operation is (Ho and Huang *et al*., 2011):

$$T_{write} = \left|\frac{(\beta D)^2}{2\mu_v(\beta-1)V_{write}\ R_{OFF}^2}\ x\ (R_{OFF}^2 - R_{ON}^2)\right| \quad (3)$$

In contrast, a read operation requires shorter time duration$T_{read}$ than the write operation$T_{write}$ ; this short time is used to alleviate too much change in the memristor internal state that might lead to soft errors (Ho and Huang *et al*., 2011).

***Fault analysis and test:***

This section reviews the fault analysis and test of RRAM presented in (Haron and Hamdioui, 2011), (Haron and Hamdioui, 2012). These two published literatures motivate the work presented in this manuscript. The section also explained the limitation of a test approach presented in (Haron and Hamdioui, 2012).

In (Haron and Hamdioui, 2011), a defect injection and circuit simulation was carried out using SPICE tools to analyze the faulty RRAM cell behavior in the presence of defects. Open defects were considered in this manuscript as this defect type is expected to have high occurrence probability in RRAM (Strukov and Likharev *et al*., 2008), (Strukov and Likharev, 2007). The fault analysis showed that not only the traditional memory fault models such as Transition Faults ($TF_1$and$TF_0$), Stuck at Faults ($SAF_1$and $SAF_0$) and Incorrect Read Faults ($IRF_1$) (Hamdioui and Van Der Goor, 2000) exist, but also new unique ones. The new unique ones are referred to as Undefined State Faults (USF) as follows:

- $USF_0$– The cell is set to an undefined state by a write 0 operation. The top two curves in Fig. 4 reflect the consequences of this problem. Open resistances $19k\Omega \leq R_{op} \leq 56\text{k}\Omega$ shift the state of the undefined state $0.4 \leq \frac{w(t)}{D} \leq 0.6$.
- $USF_1$– The cell is set to an undefined state by a write 1 operation.

Undefined State Faults (USF) cause impacted cells return to a random logic valuewhen the cell is read. Using sequence of write and read operation of march testscannot guarantee the detection of such faults. This is because march tests are basedon sensitizing cells under test (CUT) at nominal voltage value (i.e., $GND$ for$w0$ and$V_{dd}$ for $w1$). Hence, the detection of these faults requires stressing the cell in such a way that: (i) the state of faulty cells will be shifted from the undefined toa wrong state and (ii) the state of fault-free cells remains in their correct state. Animmediate read operation following the stressing will detect the faulty cells.

The properties of RRAM operation – time and voltage – were manipulated inorder to develop the appropriate test scheme (Haron and Hamdioui, 2012). Reducing one of these propertieswhile keeping another one at nominal value results in a test stress (also known asweak write operation). The strength of the weak write operations was determinedby setting the target open defect value that sets the RRAM cell to reach a certainboundary. For example, the proposed Low Write Voltage (LWV) DfT schemeapplies $V_{LWV} = 0.64$for the nominal write duration able to detect$USF_0$. Fig. 4shows that the states of the faulty cell with the target open resistance$R_{op} > 19k\Omega$ are shifted from the undefined state to logic 1 by the weak operation $\widehat{w}1$; hence thefaulty cell is detected when it is read.

Despite detecting the targeted open defects, the LWV scheme is designed at thepre-fabrication stage. Because of process variation, it is difficult to define accuratecritical defect values, which in turn will be used to set the appropriate voltage levelsfor the LWV scheme. As these DfT schemes apply weak write operations at a fixed strength, which is determined based on to the best available pre-fabrication data,they might either understress or overstress the cells leading to test quality and costissues.

As shown in Fig. 4, there is a problem with the LWV scheme when, e.g., processvariations cause most of the RRAM cells are impacted by $R_{op} = 18k\Omega$, insteadof the target $R_{op} = 19k\Omega$. In this scenario, the weak write operation performed bythe LWV circuit only shift the internal state$\frac{w(t)}{D}$,of the defective RRAM cells toonly 0.59, which is an undefined state. Therefore, these cells might escape the testalthough DfT schemes are used; this leads to the same test quality and overkillproblems as that of functional tests. Redesign may solve this problem, yet this processimposes extra time and cost (Pavlov and Azimane *et al*., 2005). Therefore, the single-stress DfT schemesmust be modified so that they can be adjusted digitally for different stress settings.

To tackle these limitations, both the DfT schemes must be modified so thatthey can be adjusted for different settings that suit the targets. The following sectionintroduces an improved DfT scheme aimed to solve the limitation of the DfTschemes proposed (Haron and Hamdioui, 2012).

***Proposed programmable DfT scheme:***

This section introduces the proposed testscheme including the concept, design methodology and test strategy. Note that this DfT scheme is based on multiple-level of voltages applied on the memory cell under test.

Regardless of the defect values, the weak write operation of the LWV scheme shifts the state of the cell at a fixed distance (i.e.,$\frac{w(t)}{D} = 0.2$). This is the reason behind its limitation to detect faults due to process variation as mentioned before. If now the scheme is extended to have multiple voltage values that can be programmed, one of the resulting electrical field shifts can be selected to shift theRRAM cell to a desired defined state. For example, if the weak operations are applied at$V_{LWV} = 0.36V$ and$V_{LWV} = 0.37V$, the cell statewill be shifted to

$\frac{w(t)}{D} = 0.59$ and $\frac{w(t)}{D} > 0.59$, respectively. Hence, using multiple supply voltage values (weak write settings) enable a cell having different defect values to be shifted to the defined state when the appropriate setting is applied.

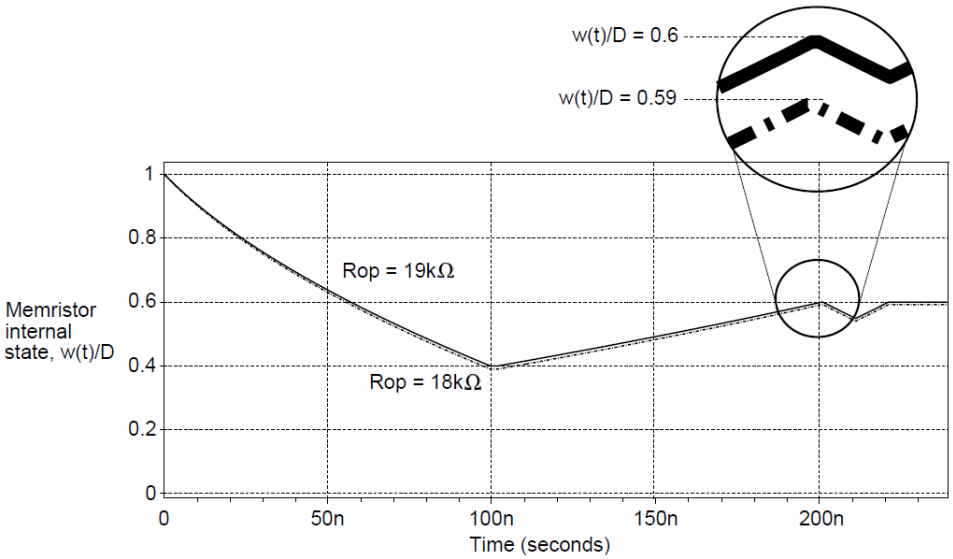


**Fig. 4:** Simulation results that show the limitation of LWV scheme for $1w0\hat{w}1r0$.

Fig. 5 shows different weak write settings where several reduced write voltages $V_{LWV0}$ are applied at a nominal time duration $T_{write}$ when test mode is activated.The selection of the appropriate $V_{LWV0}$depends on the p-bit Selection signals. This scheme is referred to as *Programmable LWV (PLWV)* scheme. Note that there is a trade-off between the precision of test stress settings and implementation overhead when choosing the $p$ values. Bigger $p$ values result in better precision but require more complex circuit.

As already mentioned, this scheme is based on reducing the supply voltage $V_{dd}$ while keeping the nominal write access time $T_{PLW}$. Identifying the supply voltage level of weak write is crucial; it has to detect faulty cells but at the same time prevent overkill. To accomplish this, three steps are utilized as follows.

1. Set the p cell state boundaries that the PLWV scheme has to shift to a defined state. As a case study, $p = 2^4 = 16$ is used to have a sufficient precision at an acceptable area overhead cost. In addition, only memory sequence initial cell to 1, write 0, weak write 1, read 0 ($1w0\hat{w}1r0$) is considered. The low state boundary $B_{low}$ can be represented by 16 possible $\frac{w(t)}{D}$ points between $B_0 = 0.45$ and $B_{015} = 0.3$ with 0.01 steps. This boundary range ensures that not only the faulty cells that might enter the undefined state (quality problem) will be detected, but the ones that cause in-field failures (reliability problem) as well.

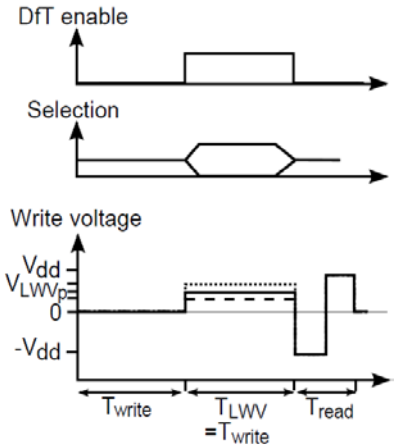


**Fig. 5:** Control signals for the PLWV scheme.

2. Search for the 16 critical open defect$R_{cr}$ values that produce each targetedboundary state. For this step,open defects with various resistance values $1k\Omega \leq R_{op} \leq 100k\Omega$ are injected within the RRAM cell and $^{1w0}$ sequence is performed.
3. Search the required time for DfT scheme by performing memory operations 1w0w1 to the RRAM cell injected with the critical $R_{op}$ value determined in Step 2. Fig. 6 shows the SPICE simulation results for $T_{LWVp}$ where 16 different $\frac{w(t)}{D}$ curves change in accordance to the write voltage level applied on the cell. Each $\frac{w(t)}{D}$ curve shifts in its own path corresponding to the respective $R_{op}$ values injected; e.g., the bottom $\frac{w(t)}{D}$ that shifts from 1 to 0.3 and back to 1 corresponds to $R_{op} = 9.88k\Omega$. The voltages obtained from the simulation are between $V_{LWV\,0} = 0.53V$ to $V_{LWV\,15} = 0.84V$, as shown in the figure.

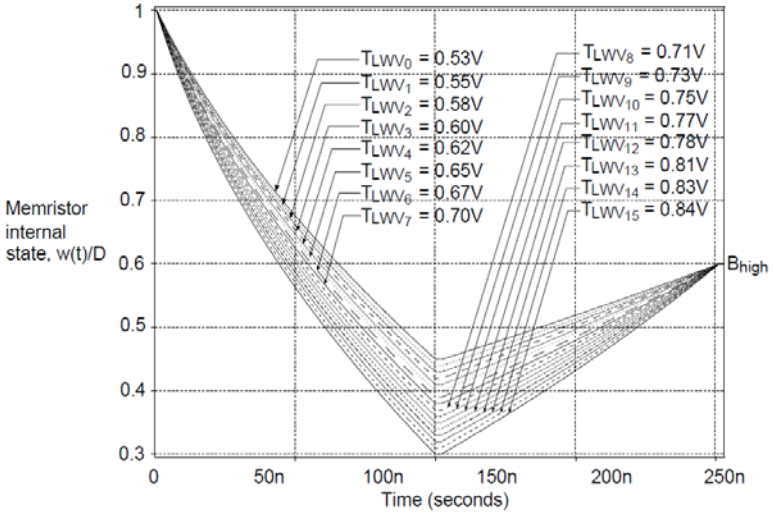


**Fig. 6:** Simulation results of multiple voltages for PLWV scheme.

Clearly, the PDfT schemes provide higher fault detection capability than DfT schemes; this is because the PDfT schemes perform iterative processes, each of which using different test stress settings. However, these schemes require a long test time. To address this problem and at the same time retaining the fault detection capability at an acceptable level, an appropriate test strategy is required as follows.

1. Set to one of the p different test stress settings.
2. Perform the following steps for all n RRAM cells.
a. Initialize memory cells to 0.
b. Write 1 to memory cells.
c. Activate the PLWV circuit and apply weak write 0; only defective cells will flip to 0.
d. Deactivate the PLWV circuit and read 1 from the cells. If the read value is 0, then faults are detected.
e. Initialize the cells to 1.
f. Write 0 to the cells.
g. Activate the PLWV circuit and apply weak write 1; only defective cells will flip to 1.
h. Deactivate the PLWV circuit and read 0 from the cell. If the read value is 1, then faults are detected.
3. Check the desired fault coverage for n test signatures.
a. If the fault coverage is not satisfied, check whether all p settings havebeen applied. If “no”, then change the test stress settings so that adifferent weak write value will be applied in the next test iteration; and go to Step 1. If “yes”, then go to Step 4.
b. If the fault coverage is satisfied, then perform appropriate actions (e.g.,self-repair or reconfiguration of sparing cells) to defective RRAMcells.Go to Step 4.
4. Save the last test stress setting for future testing.
5. Stop testing.

***Evaluation results:***

This section gives evaluation results of the proposed programmable DfT scheme. The section starts with the simulation set up and results followed by the proposed DfT circuit.As a case study, the 16 stress settings obtained earlier were applied to the memory cell under test in SPICE simulation environment. Each time a critical single open defect is injected into the SPICE memory model and the simulation was performed.

Fig. 7 shows the simulation results for the PLWV scheme when it is programmedto one of the 16 weak write durations, i.e., based on $R_{cr} = 17.93k\Omega$ that requires $V_{LWV6} = 0.67V$. The figure shows that for $R_{op} = 19k\Omega$, the state of the cell is shifted to the incorrect logic 1 state instead of the undefined state as it is for the LWV scheme. As the state of the cell is now shifted to a defined state, the read operation detects the faults. Note that different fault coverage can be obtainedusing different weak write settings.

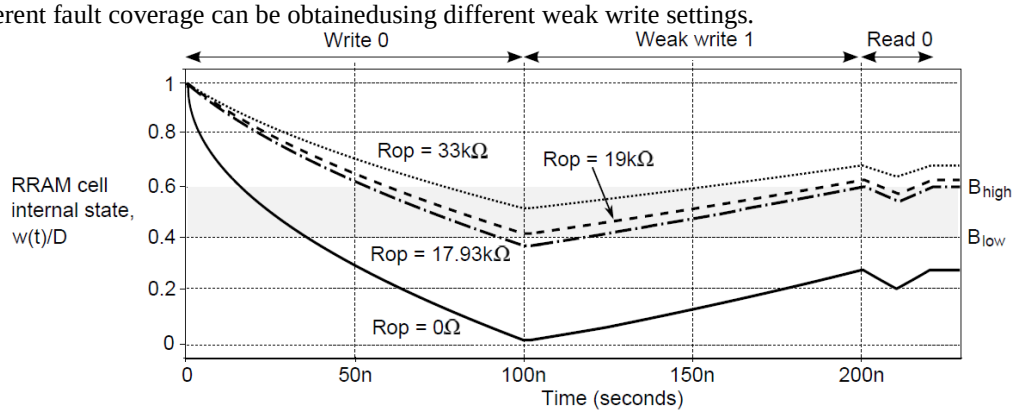


**Fig. 7**: Simulation results of PLWV scheme for $V_{LWV6}$.

To have the programmable capability, the DfT scheme must be incorporated with the appropriate facility. As shown in Fig. 8, PLWV circuit consists of a decoder, and a voltage divider circuit formed by multiple transistors and parallel resistors. When the $DfTE$ signal is set to low, $M_{17}$ is switched on and the normal operation is performed. At the same time, the decoder is deactivated and $M_{16}$ is switchedoff. When the $DfTE$ signal is set to high, the PLWV operation is activated where the four selection signals $S_1$ to $S_4$ will select the appropriate transistors $M_{16}$ to $M_{15}$. At the same time, transistor $M_{16}$ is switched on to supply $V_{dd}$ to the voltage divider circuit. The activated transistor (one of transistors $M_0$ to $M_{15}$) allows its corresponding voltage divider circuit to supply a reduced voltage $V_{LWVp}$. For example, when $S_1S_2S_3S_4 = 1111$, the $Wk_{15}$ signal is activated to switch transistor $M_{15}$ on; this in turn supplies $V_{LWV15} = V_{dd}\ x\ \frac{R_{31}}{R_{30}+R_{31}}$. for the weak write operation. Table 1 gives the values of the resistors used to structure the voltage divider circuit where $V_{dd} = 1.5V$ an $R_1 = R_3 = R_5 = \ldots = 1k\Omega$. Different appropriate resistor values can also be used that satisfy the output voltage.

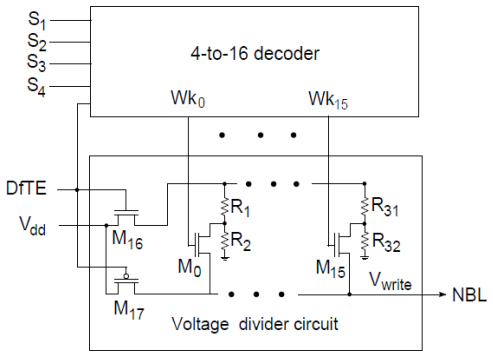


**Fig. 8:** PLWV circuit.

**Table 1:** Resistances for the divider circuitries in PLWV circuit.

| $p$ values | Resistance (Ω) | | $p$ values | Resistance (Ω) | |
|---|---|---|---|---|---|
| 0 | $R_1 = 1k$ | $R_2 = 546$ | 8 | $R_{17} = 1k$ | $R_{18} = 899$ |
| 1 | $R_3 = 1k$ | $R_4 = 579$ | 9 | $R_{19} = 1k$ | $R_{20} = 948$ |
| 2 | $R_5 = 1k$ | $R_6 = 630$ | 10 | $R_{21} = 1k$ | $R_{22} = 1k$ |
| 3 | $R_7 = 1k$ | $R_8 = 667$ | 11 | $R_{23} = 1k$ | $R_{24} = 1.055k$ |
| 4 | $R_9 = 1k$ | $R_{10} = 705$ | 12 | $R_{25} = 1k$ | $R_{26} = 1.083k$ |
| 5 | $R_{11} = 1k$ | $R_{12} = 576$ | 13 | $R_{27} = 1k$ | $R_{28} = 1.174k$ |
| 6 | $R_{13} = 1k$ | $R_{14} = 807$ | 14 | $R_{29} = 1k$ | $R_{30} = 1.239k$ |
| 7 | $R_{15} = 1k$ | $R_{16} = 875$ | 15 | $R_{31} = 1k$ | $R_{32} = 1.273k$ |

***Conclusion:***

This manuscript presented a programmable Design-for-Testability (DfT) schemeto improve the detection of faulty RRAM cells due to open defects that caused by variations during fabrication processes. The proposed DfT scheme is based on multiple values of weak write voltage applied to the nominal write duration; thus, is referred to as Programmable Low Write Voltage (PLWV). The manuscript begins with an overview of the

RRAM functional model, electrical model and operations. Thereafter, a brief description of the related published literatures that motivate the work in this manuscript has been discussed. Next, the limitation of the existing DfT scheme to deal with process variation-induced defects, which cause faults with different defect values, is explained. Finally, the PLWV scheme has been introduced including the concept, design methodology, test strategy, circuit and simulation results. The proposed scheme is able to detect faulty RRAM cells that are impacted by different open defect values by adjusting the weak write voltages. Therefore, PLWV provides a better fault detection capability and in turn improve the fault coverage than the state-of-the-art. Future work focuses on the evaluation and remedy for other defect types such as bridges that impacts adjacent RRAM cells.

## ACKNOWLEDGMENT

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