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Pragmatic Corroboration of Time Shared Cyclic Switching HPWM in Three-Phase Inverter

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ABSTRACT

Background: The sinusoidal pulse width modulator (SPWM) is the most used method of pulse width modulation (PWM) in dc-ac power conversion equipment. In SPWM techniques, the switches are commutated at high frequency, as higher the carrier frequency lesser the filtering difficulty. However, During a typical turn–on and turn-off, the device undergoes high power loss, which increases linearly with the switching frequency. Time shared cyclic switching hybrid pulse width modulation (TSCHPWM) method improves circuit reliability through thermal equalization of all the six switches in a HPWM three-phase inverter, while retaining reduced switching losses, the inherent ease of filtering and output quality. **Objective:** To improve thermal management, a time shared cyclic switching HPWM method for MOSFET based three-phase dc-ac converter is demonstrated in hardware. **Results:** Simulation and hardware studies clearly reveals that the switches in the converters operate at low temperature compared to conventional PWM, thereby increasing the reliability and life expectancy of the switches. Electro-thermal modeling and estimation of inverter losses gives the designer an idea to attach proper thermal management device i.e. cooling device to semiconductor. **Conclusion:** The proposed method has its significance usage in reliability enhancement of high power-continuous rated inverter drives designed with Intelligent Power Modules (IPM). The TSCSHPWM allows use of identical power devices and heat sinks, permitting a simpler, more reliable design.

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INTRODUCTION

The sinusoidal pulse width modulator (SPWM) based on sine-triangular method is perhaps the most used method of pulse width modulation (PWM) in dc-ac power conversion equipment. It forms an integral part of a wide range of control systems: open loop V/Hz drives, current or voltage regulated vector drives, regenerative converters, uninterrupted power supply (UPS), static VAR compensators, harmonic filters, and many other types of single/poly-phase dc-ac power converters (Boost, M., P.D. Ziogas, 1986; Michael A. Boost 1998; Antar, R.K., 2012; Ali Dastfan, 2000). The 180^0 and 120^0 modes of SPWM schemes are popularly known in three-phase applications. Device manufacturers started integrating power devices and related accessory components as intelligent power modules for PWM requirements for various applications. In SPWM techniques, the switches are commutated at high frequency, as higher the carrier frequency lesser the filtering difficulty. During a typical turn–on, the voltage across each power device changes to very less voltage (on-state drop) from the voltage level which is nearly equal to the dc input voltage, in a short duration (t_{on}). At the same time, current through the device transits from leakage level to high value. Similarly, during turn-off, voltage and current transients will be in reverse manner. Consequently the device undergoes high power loss, which increases linearly with the switching frequency. In other word, the power switches dissipate a considerable amount of heat and scarify the circuit efficiency. To achieve high power densities in a practical design, high power conversion efficiency is a basic requirement (Allen Hefner, 2004).

The probability of failure in electronic systems is strongly dependent on the operating temperature as shown in the Fig. 2. Thermal overstress is the most common failure cause in modern electronic systems. Thus long-term reliability consideration requires operation at low junction temperature. Therefore, reliability should be considered carefully for design. Majority of industries favor the concept of reliability-driven design rules. It is noted that reliability simulation can lead to development of less conservative design rules.

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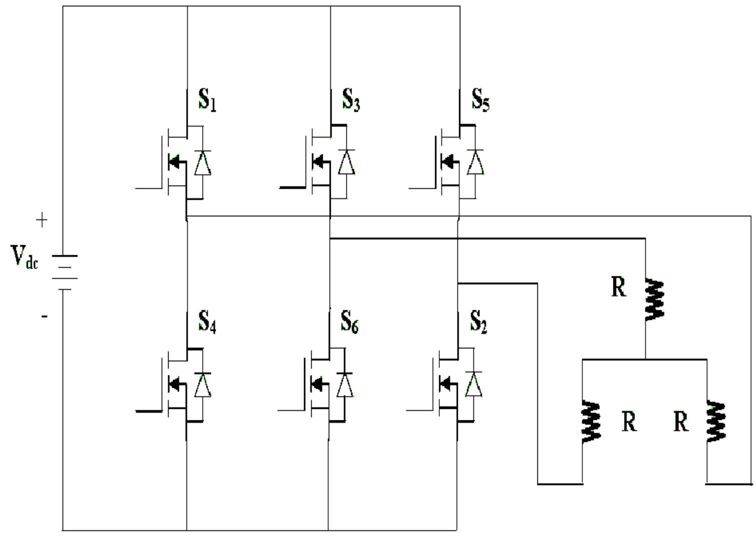

Fig. 1: Basic three–phase inverter with resistive load.

Accordingly, soft switching inverters have been proposed in recent years greatly decreasing switching loss (Lai, J.S., 1997). However, it requires auxiliary switches and diodes with (sometime) higher rating than that of main switches. Additional soft switching problems include duty ratio limitations and load type restriction. An additional alternative is Hybrid PWM (HPWM) method, where a high-quality output waveform can be obtained without significant switching loss penalty (Ray-Shyang Lai, 1995). In this method, three of the six switches are pulse width modulated at high frequency for high-quality output, and the other three are commutated at the (low) output frequency to reduce switching losses. Thus, conventional HPWM design requires the use of different devices and/or heat sinks to handle switch temperatures. Not only need the sink temperature of the upper switches be reduced, the junction temperature must be limited to keep switch operating in safe operating area (SOA). Using the same switch but with different heat sink, junction temperature must be different even if the sink temperature are equivalent (Keskar, N., 1999). Although the total switching loss is reduced in HPWM, the switching losses of the six switches are unequal especially at high frequency. This causes excessive heating at the high frequency switches, thereby sacrificing their life fast and hence reliability of total circuit degrades because of non-uniform utilization. On the other hand lower switches, working at reduced power dissipation and temperature, have better life and switches generating problems of practical design.

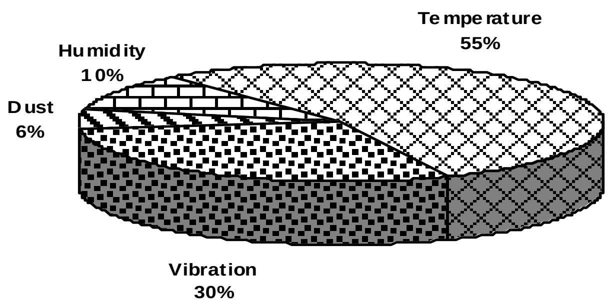

Fig. 2: Major causes for electronic failure.

In order to overcome this problem, hybrid switching HPWM (HSHPWM) have been proposed for single-phase H-bridge inverter and experimentally verified (Tsu-Hua Ai, 2001). The preliminary idea of the time shared cyclic switching hybrid pulse width modulation (TSCHPWM) has been given in (Shenai, K., 1991), which is conceptually similar with HSHPWM while procedurally different. TSCHPWM has thermal equalization time cycle (TETC) equal to the period of output voltage while TETC of HSPWM is twice that of TSCHPWM (Keskar, N., 1999). Both HSHPWM and TCSHPWM methods equalize switching losses and heating among the switches; thereby the thermal management and reliability of system can be improved. These methods have the same frequency spectrum as the conventional SPWM and switching losses as the HPWM. The concept of TSCHPWM has been healthy extended to three-phase inverter 180^0 mode of operation and simulated results are presented (Kan Berringer, 2003).

The aim of this paper is hardware verification of TSCHPWM method for power MOSFET based three–phase inverter circuit for wide range of frequency. The experimental verification uses Fluke 80T-150U universal temperature probe for temperature measurement. ICAP simulation packages' energy loss curves for power switches are also presented.

TSCHPWM Topology:

In the TSCHPWM method, the switches are commutated at high and low frequency in time-sharing mode at each cycle of the output. The time duration of both high and low frequency operations are chosen such that for all switches total duration of high frequency operations and low frequency operations are same. The difference in the TSCHPWM scheme with conventional HPWM is all upper devices are commutated at carrier frequency for first 90° of conduction and next 90° of conduction at low frequency.

Table 1: Firing Chart.

Conduction period	Upper switch	Lower switch
	S_1	S_4
(0-90)	High	OFF
(90-180)	Low	OFF
(180-270)	OFF	Low
(270-360)	OFF	High

In case of lower group, devices are commutated at low frequency for the first 90° of conduction and at carrier frequency for last 90° of conduction. For easy understanding of TSCHPWM scheme, the firing sequence for R-phase (first arm in the inverter bridge) is given in Table 1. Firing sequences for remaining two phases are also in fashion but phase shifted for 120^0. The complete set of gate pulses for the TSCHPWM topology is shown in the Fig.3. The gate signal period for all six switches over the total gate signal period is similar, and thus, total power losses (Williams, B.W., 1992; Alan Mantooth, H. and Allen R. Hefner, Jr, 1997; Hoon Lee, J. and Bo H. Cho, 2003) for all six switches is equalized.

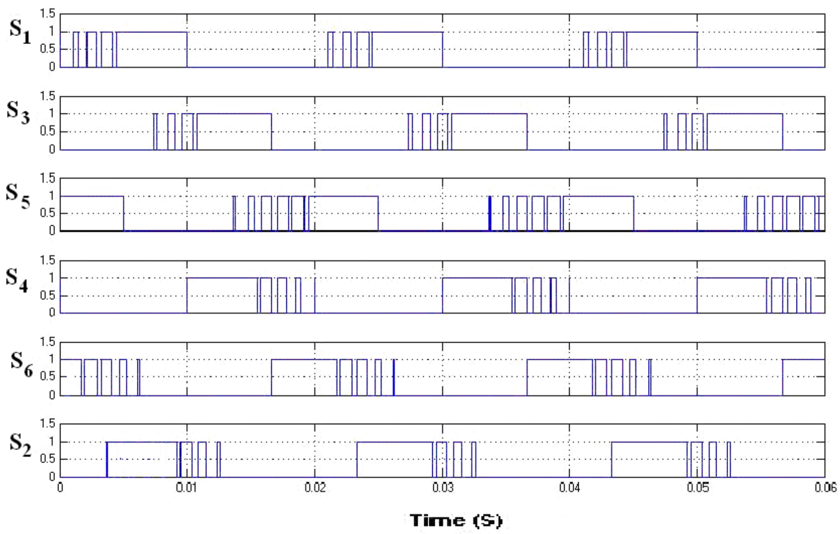

Fig. 3: Gate signals – TSCHPWM.

Simulation Study:

A THD:

The main advantage of TSCHPWM is retaining the betterments of conventional SPWM in quality aspect and HPWM in efficiency aspect. To very its spectral preserving Simulink toolbox is used. The simulated specifications were input dc voltage, V_{dc}=100V, output frequency, f_o= 50Hz, load resistance, R_L=10Ω, and various values of modulation depth, M_a and frequency ratio M_f. The representative the output waveform resulted for TSCHPWM for Ma=0.8 and M_f=30 is given in proposed topology is shown in the Fig. 4. Good agreement between the results of SPWM, HPWM and TSCHWPM methods is noticed and the comparison of THD values for few carrier frequencies are tabulated in Table 2. Simulation results also substantiate that TSCHPWM retains all the properties of SPWM.

Table 2: Comparison of total harmonic distortion.

f_{sw} (kHz)	%THD SPWM	%THD HPWM	%THD TSCHPWM
10	77.14	76	75.93
20	78.08	76.58	76.5
40	78.79	76.66	76.55

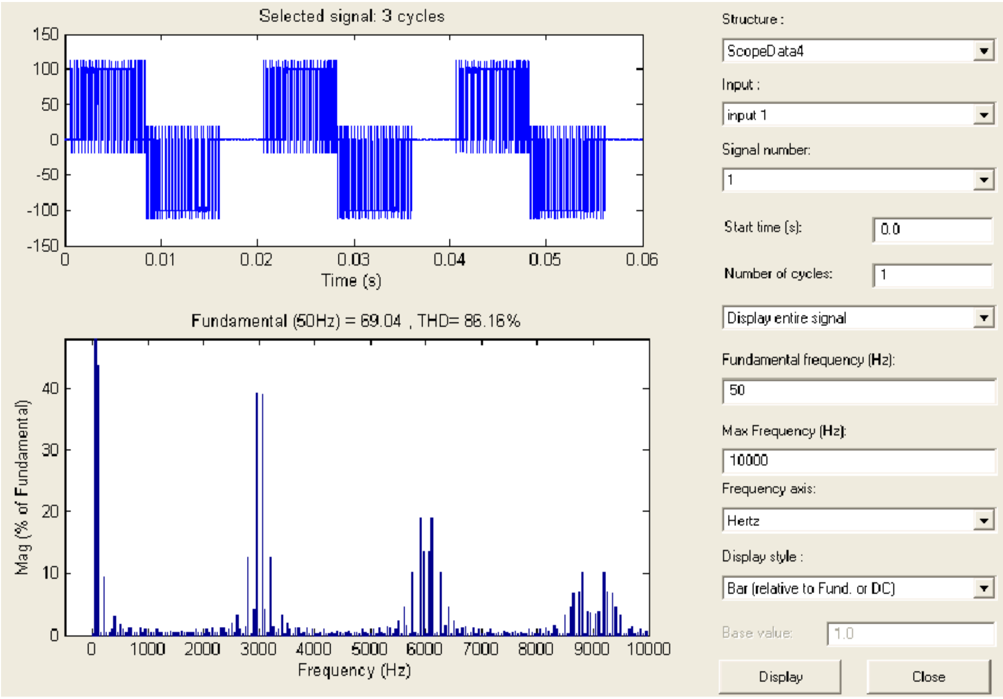

Fig. 4: Output frequency spectrum – TSCHPWM.

B. Energy Loss:

The ICAP (Intusoft, USA) circuit simulation package has been used for energy loss estimation of power switches. The energy loss curves are obtained for HPWM and TSCHPWM for inverter specifications of V_{dc}= 100V, R_L=10Ω, f_c=1kHz, M_a=0.8. Fig.5 and Fig.6 show total energy loss E_{TL} as example cases of HPWM (one upper arm switch and one lower arm switch). In TSCHPWM the energy losses in all switches are very close and the Fig. 7 and Fig.8 show the representative cases for upper arm and lower arm respectively. The total energy loss of S_1 and S_4 in HPWM is 760mJ and 68mJ where as in TSCHPWM is 440mJ for all switches (approximately).

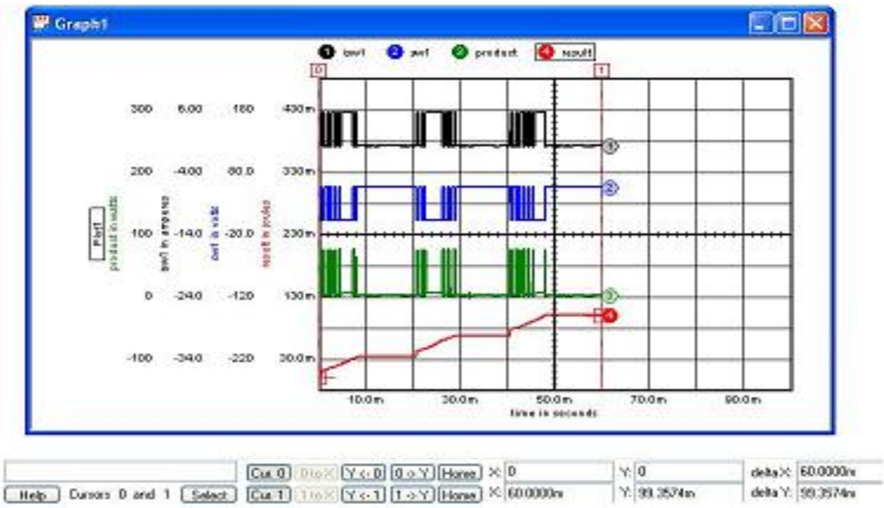

Fig. 5: HPWM - high frequency switch (S_1).

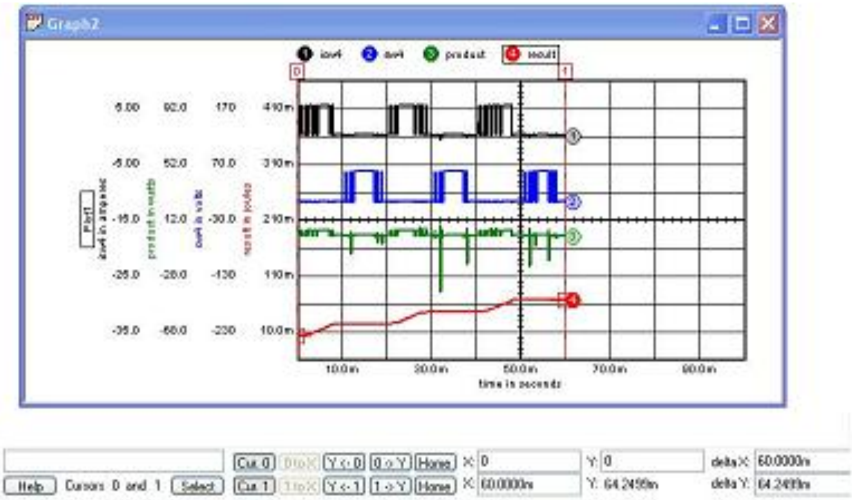

Fig. 6: HPWM- low frequency switch (S_4).

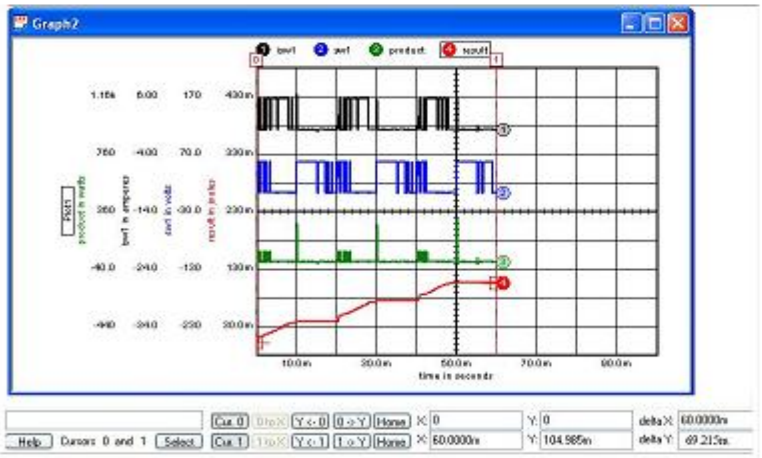

Fig. 7: TSCHPWM-upper group switch (S_1).

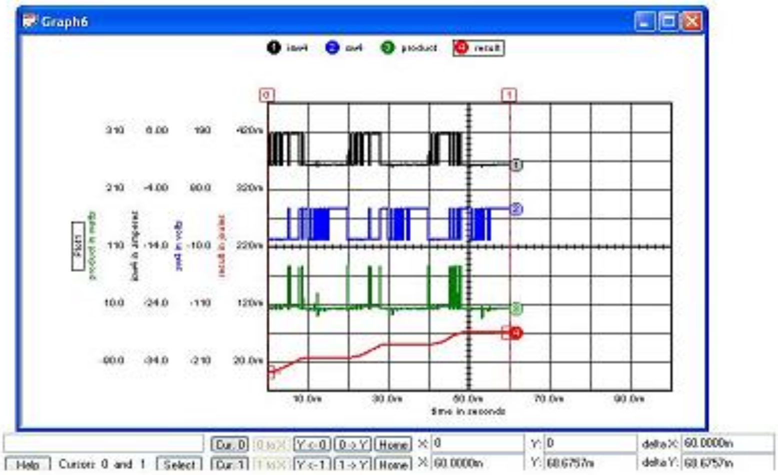

Fig. 8: TSCHPWM-lower group switch (S_4).

Experimental Results:

A three-phase inverter power circuit was built with IRF830 MOSFET to demonstrate the feasibility of TSCHPWM and comparison with the HPWM of the same general specification. The basic PWM controller is designed with XR-2206 is a function generator IC, which has the capability of generating both sine and

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triangular signals with low distortion and has frequency stability from 0.01Hz to 1MHz. Using XR2206 IC the sine and triangular waveforms are generated as shown in Fig. 9 and 10 respectively.

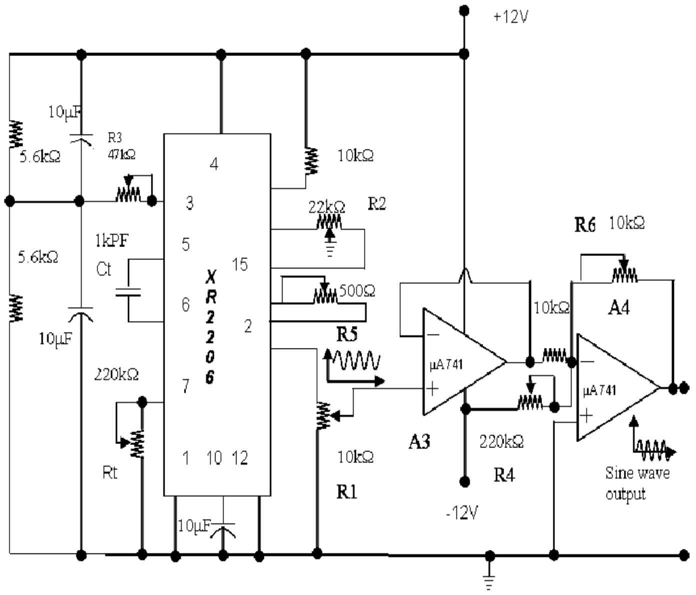

Fig. 9: Generation of reference sine.

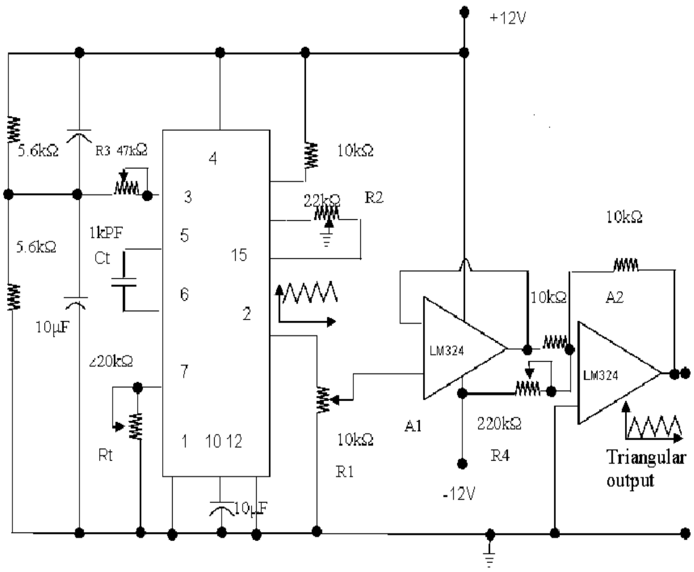

Fig. 10: Generation of triangular waveform.

The TSCHPWM gating signals are derived from the basic SPWM signals by a combinational logic circuit represented in Fig.11. The functions of the combinational logic circuit are expressed as

$$
\begin{aligned}
S_1 &= L_R M_R H_R + \overline{M_R}\, L_R \\
S_4 &= \overline{L_R} M_R H_R + \overline{M_R}\, \overline{L_R} \\
S_3 &= L_B M_B H_B + \overline{M_B}\, L_B \\
S_6 &= \overline{L_B} M_B H_B + \overline{M_B}\, \overline{L_B} \\
S_5 &= L_Y M_Y H_Y + \overline{M_Y}\, L_Y \\
S_2 &= \overline{L_Y} M_Y H_Y + \overline{M_Y}\, \overline{L_Y}
\end{aligned}
\qquad (1)
$$

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The input signals of this combinational circuit are 50Hz square wave obtained from input sine using zero crossing detector (L_R), frequency doubled signal of L_R (M_R) and PWM signal obtained from comparison of carrier-triangular and 50 Hz sine-reference (H_R). The suffixes R, B and Y are to represent R phase, B phase and Y phase respectively. The inverted signals to L_R and M_R are generated internally. Fig.12 shows the various signals involved in the logical expression (1) as functional block. To simplify observation of the waveforms, a relatively low carrier frequency of 1 kHz is used. The photograph of the constructed hardware is shown in Fig.13.

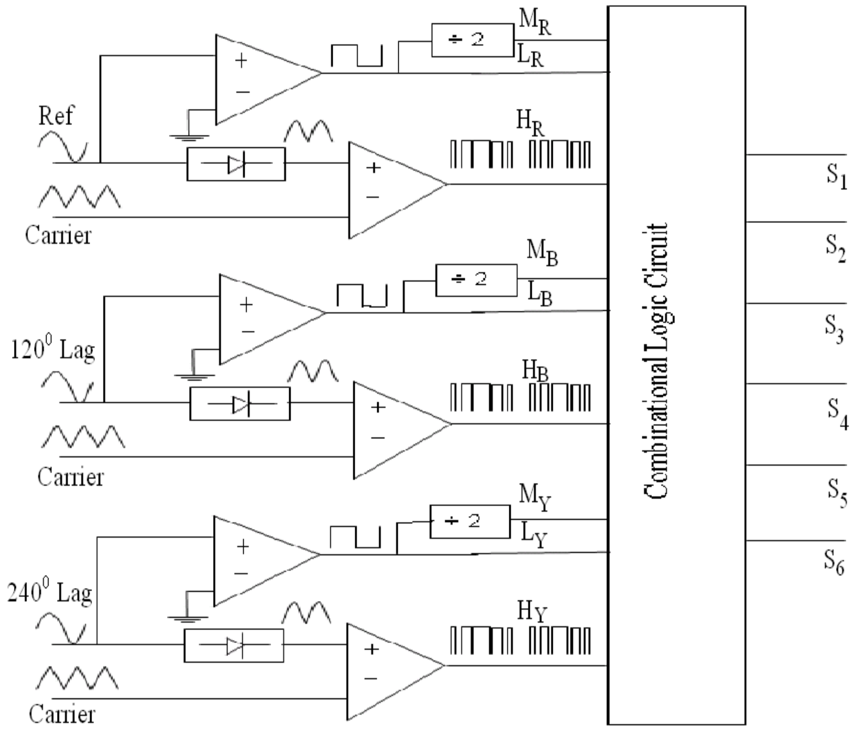

Fig. 11: TSCHPWM gate signal generation.

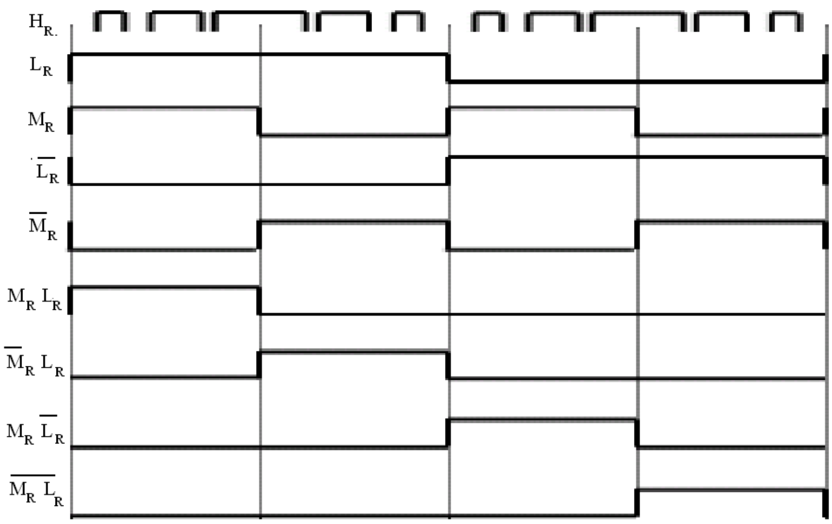

Fig. 12: Signals associated with R phase.

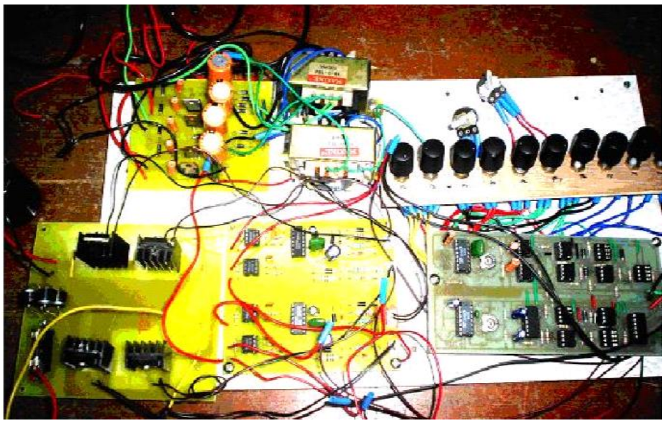

Fig. 13: Hardware set up.

The heat sink temperature rise is measured by exposing the probe (80T-150U universal temperature probe) tip to the sink attached to the device. Fig.14 shows temperature of heat sink in various switches of both HPWM and TSCSHPWM inverters at different carrier frequencies. In TSCSHPWM, all switches are working with same value of temperature while in HPWM, the upper arm switches temperature raises with operating frequency while lower arm switches has constant, minimum temperature as they are commutated at output frequency always. Thus, TSCSHPWM combined merit of both SPWM and HPWM is confirmed.

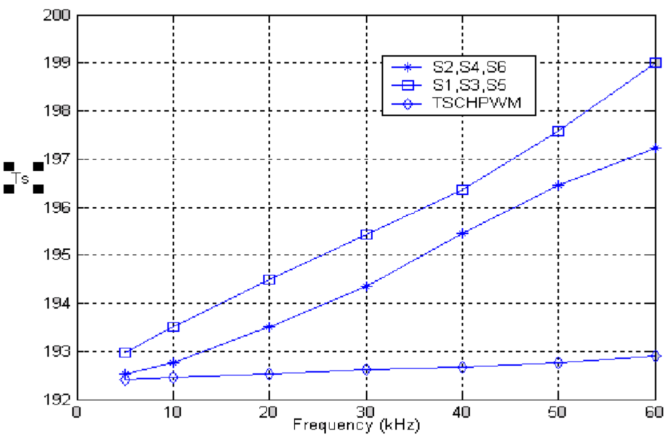

Fig. 14: Experimental heat sink temperature rise.

Conclusion:

A time shared cyclic switching HPWM method for MOSFET based three-phase dc-ac converter is demonstrated in hardware to improve thermal management. Simulation and hardware studies clearly reveals that the switches in the converters operate at low temperature compared to conventional PWM, thereby increasing the reliability and life expectancy of the switches. Electro-thermal modeling and estimation of inverter losses gives the designer an idea to attach proper thermal management device i.e. cooling device to semiconductor. The TSCSHPWM allows use of identical power devices and heat sinks, permitting a simpler, more reliable design. The proposed method has its significance usage in reliability enhancement of high power-continuous rated inverter drives designed with Intelligent Power Modules (IPM).

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