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Design and Implement the Bondwire Inductors for Switching Power Amplifier

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ABSTRACT

Background: Most of the switching power amplifiers (PAs) are employed on-chip spiral inductors for matching and loading purpose. However, on-chip spiral inductors have low quality factor (*Q*) owing to high substrate loss and high parasitics. In addition, spiral inductors occupy a large space on-chip and also encounter self-resonance in microwave frequency band, which permits their use beyond that frequency. Therefore, high efficiency and smaller chip area of power amplifiers are difficult to obtain. **Objective:** The main objective of design and implement the bondwire inductors for switching PA are to obtain high Q thus a high output power and a high efficiency with the smallest chip area. **Results:** The simulated results for bondwires indicate that the values are equivalent to 2.0 nH for the 2-mm bondwire and 4.1 nH for the 5-mm bondwire. Furthermore, the implementation of bondwire inductors in switching PA indicate that the PA delivers 23 dBm output power and 44.5% power added efficiency with 3.3 V power supply into a 50 Ω load with the chip area is 0.37 mm². **Conclusion:** The proposed bondwire inductors and implementation in a switching power amplifier shows that power amplifier obtain good output power and efficiency with the smallest chip area.

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INTRODUCTION

The main objective of design and implement the bondwire inductors for switching power amplifier (PA) are to obtain a high output power and a high efficiency. However, as the down-scaling of MOS devices continues, the CMOS PA is not the optimum technology of choice due to the problem such as low oxide breakdown voltage, low current drive capability, substrate coupling, and low quality and high tolerances of on chip passives (A.Mazzanti et. al., 2006, Kyu Hwan An et. al., 2008). This makes CMOS PA design and implementation a major challenge particularly when designing in GHz frequencies range.

Most CMOS PAs that are published choose differential topology to obtain high linearity watt range (Riccardo Brama et. al., 2008). Since the components driven by the PA and the antenna input are still single-ended, such topology still requires a balun or transformer to be integrated in differential topology (Riccardo Brama et. al., 2008, P. Reynaert and M.S.J Steyaert, 2007). Therefore, the design become complicated and occupies large size on chip. In CMOS, Switching class E PA is the most favored candidate among all classes of switching mode power amplifiers (Class D & Class F) due to their circuit simplicity and excellent power added efficiency (PAE) (Jun Tan et. al., 2012, Sira. D et. al, 2010). High PAE are important because PAs typically dominate the power consumption in a wireless transceiver system. However, the linearity is very poor due to the switching nature. Therefore, the systems with constant envelope modulation scheme such as FSK (or FM) are most suitable for switched-mode amplifiers.

Furthermore, signal swing in a Switching class E PA can be two or three times the supply voltage that seriously stresses MOS devices. Safe device operating conditions can be guaranteed by decreasing supply voltage which is usually less than the maximum available, at the price of efficiency degradation (K.C.Tsai and P.R. Gray, 1999, K.L.R. Mertens and M.S.J. Steyaert, 2003). Cascode configuration have been used to overcome device stress problem in MOS devices (A.Mazzanti et. al., 2005). However, a conventional cascode amplifier, the gate of common gate (CG) transistor is directly connected to the supply voltage by means extra bond pad is required (A.Mazzanti et. al., 2006).

In this paper, the bondwire inductors are realized for high Q inductors and used in a 2.4 GHz switching class E PA using 0.13-µm CMOS process. The proposed PA design employed single-ended topology with a self-biasing technique is implemented to overcome the device stress and to decrease the additional bond pads

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requirement. The driver stage is biased in Class A and the effects of bonding wires are taken into account in the simulation.

Bondwire Inductors Design Method:

CMOS on-chip spiral inductors are well known for their low Q owing to high substrate loss and high parasitics (A. Grebennikov and N.O. Sokal, 2007). Furthermore, spiral inductors occupy a large space on-chip and also encounter self-resonance in microwave frequency band, which permits their use beyond that frequency. Therefore, bondwire inductors are used in this design to implement high Q inductors to obtain a higher PAE.

Although bondwire inductors provide a high Q, predetermination of bondwire inductance is difficult. Since the inductance is sensitive to bonding geometry, the bondwires need to be modeled accurately before they can be used as inductors in a power amplifier. To obtain an accurate model, all the elements used in the inductor model need to be well defined, and modelled according to the electromagnetic theory and their physical structure. Figure 1 shows a lumped element model for a bondwire inductor. The model consists of the inductances and resistances of a bondwire caused by skin effects.

In this proposed design, two types of bonding wires with a length of 2 mm and 5 mm are used. These bondwire inductors were first simulated using Cadence SpectreRF. The Z-parameter simulation result for both bondwires is shown in Figure 2. The real parts for both bondwires are zero, while the imaginary parts are 30 and 62 for 2-mm and 5-mm bondwire, respectively, at 2.4 GHz. The values are equivalent to 2.0 nH for the 2-mm bondwire and 4.1 nH for the 5-mm bondwire.

The simulation model of a bondwire inductor gained high Q, as shown in Figure 3. This high Q resulted in the high performance of the proposed Switching class E PA. The Q for the 2-mm and 5-mm bondwires were found to be approximately 62 and 35, respectively, at the 2.4-GHz operation frequency.

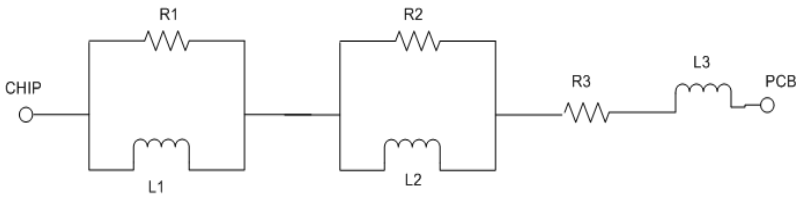


Fig. 1: Lumped-element model of a bondwire inductor.

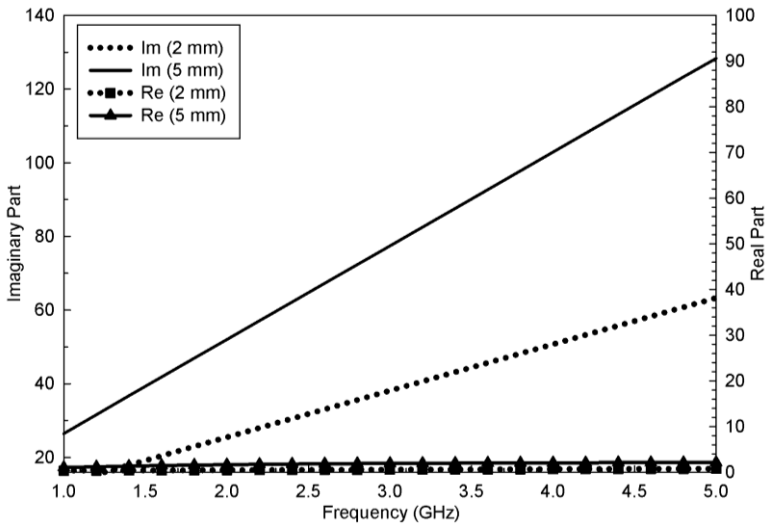


Fig. 2: Z-parameter for bonding wire inductor model.

Bondwire Inductors Implementation:

The proposed bondwire inductors integrated with switching class E PA is shown in Figure 4. The designed PA can be divided into two stages, driver stage and power stage.

The transistor of the driving stage M1 is biased in Class A with a size of 512 µm/0.35 µm. The supply voltage is set to 3.3 V. DC block capacitor C1 and bondwire L1 are part of input matching. The bondwire Ld is connected to the supply voltage (Vdd) for M1 with a length of 5 mm. The interstage matching network consists of the integrated series capacitor C2 set to 6 pF after fine-tuning to provide high gain to the power stage.

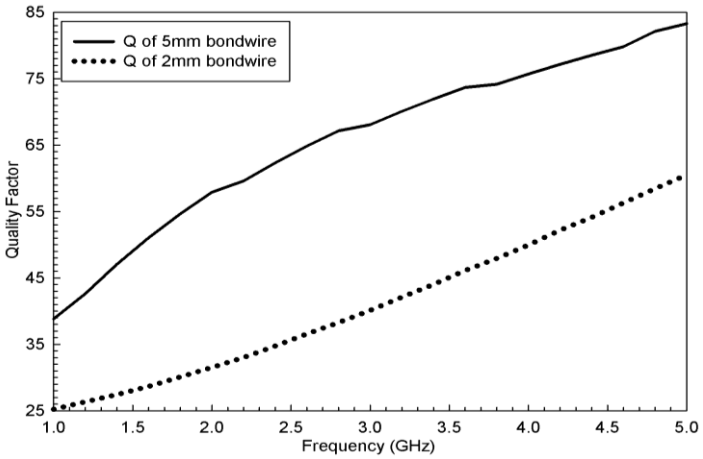


Fig. 3: Q of a bondwire inductor simulated using Cadence SpectreRF.

The power stage is implemented by cascode topology with self-bias. In the conventional Switching class E cascode topology, common source (CS) gate is connected to Vdd (1, 12). However, in this proposed design, the bias for CS gate is provided by R3 and C3, for which no extra bond pad is required. The DC voltage applied to the CS gate is the same as that applied to CS drain. The values of R3 and C3 can be chosen for optimal performance. To minimize the switch on-resistance, a maximum-size switch transistor is preferred. Thus, to optimize the performance of the power stage altogether, three transistors in parallel for CS and four transistors in parallel for common gate (CG) with 64 fingers were selected. All devices have a maximum width of 8 µm and minimum length of 0.35 µm. The gate of M2 is biased at 0.75 mV and the Vdd for M3 is 3.3 V. Based on the selected Vdd, frequency, and the desired output power, the values of Cshunt, Cs, and Ls were calculated (Phairoj Leungvongsakorn and Apinunt Thanachayanont, 2003). The finite DC inductance Ldc is realized by a 5-mm bondwire connecting the CS drain to the DC supply connection.

The 50 Ω output resistance is downconverted by means of the simple L–C matching circuit, Lo and Co. Lo is realized by 5-mm bondwire, Co being an off-chip capacitor with the value of 3.3 pF. Co is a high-frequency microchip capacitor, which has the contact on the surface side and the ground on the opposite side. Therefore, extra bondwire Lext is required to connect to the output for experimental purpose with the length of 2 mm.

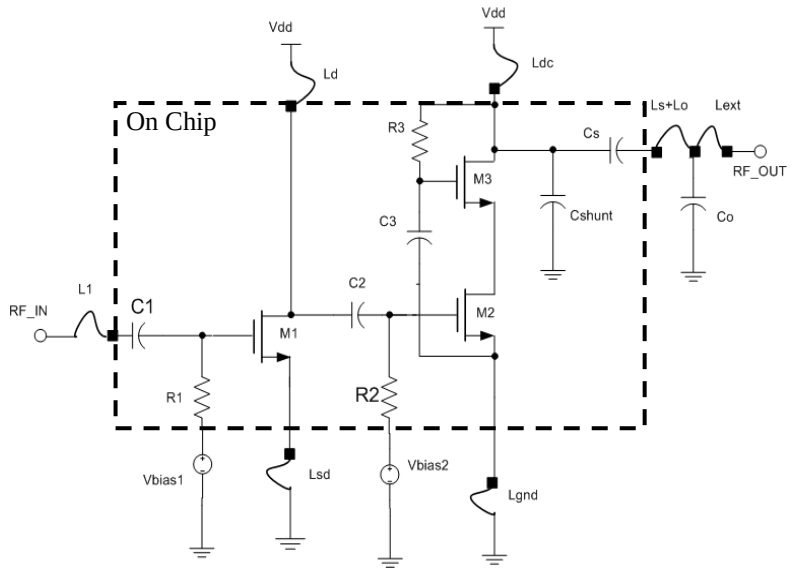


Fig. 4: Complete schematic bondwire inductors and CMOS Switching class E PA.

RESULTS AND DISCUSSIONS

The circuit design of bondwire inductors with switching class E PA is simulated using Cadence SpectreRF simulator in 0.13-µm CMOS process. Figure 5 shows the simulated drain voltage and current waveform of the power stage. Switching class E operation wherein the voltage and current are not overlapping with each other can be observed. On the other hand, the voltage and current are not maximum level at the same time, that is, the

power dissipation or the product of drain current and voltage are minimized. Therefore, high efficiency can be obtained. The minimum voltage is non-zero because of the transistor's on-resistance.

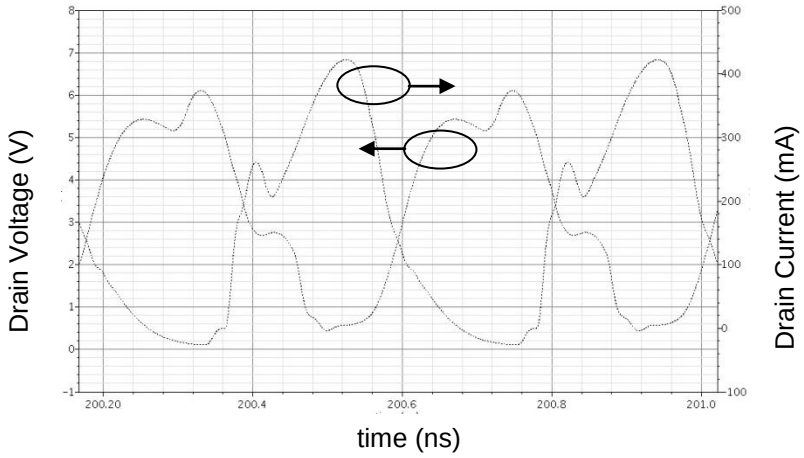


Fig. 5: Transient response for drain current and drain voltage of *M3.*

Figure 6 shows the pre-layout simulation and post-layout simulation for the output power (Pout) and PAE vs. input power (Pin). The results for the post-layout simulation are degraded because of the parasitics effects. However, both simulation results match well at higher input power levels. The proposed switching class E PA delivers the maximum output power of 23 dBm with 44.5% PAE for an input power of 16 dBm. Output power and PAE versus supply voltage are shown in Figure 7 (a), the output power changes approximately proportional to Vdd^2, from 18.5 dBm to 24.5 dBm when the supply voltage is swept from 2.0 V to 3.6 V. It can be noted that the output power can be controlled through the supply voltage. Figure 7 (b) shows the output power and PAE of the PA as a function of frequency. The output power is kept at least 20 dBm over the frequency range of 2.0–2.6 GHz. However, more than 40% of high efficiency is kept only over the frequency range of 2.35–2.50 GHz. This PA can operate at the 2.35–2.50 GHz band with higher performance. Output power and power gain versus input power is shown in Figure 8. The maximum power gain of approximately 13 dB is obtained for an input power of 6 dBm.

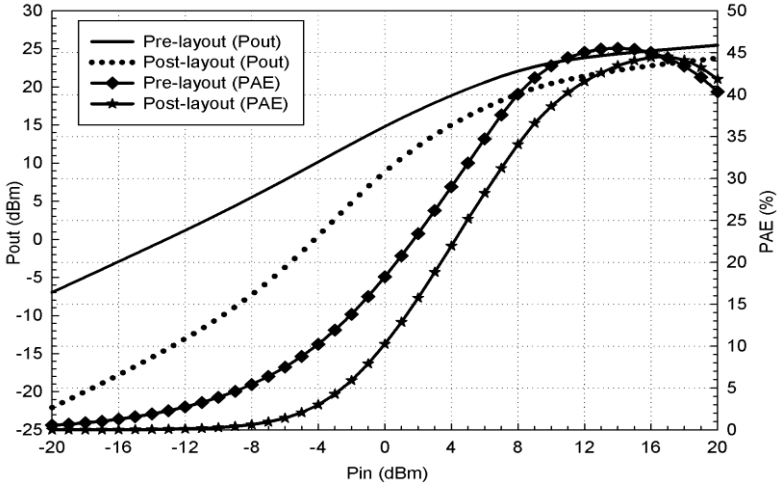
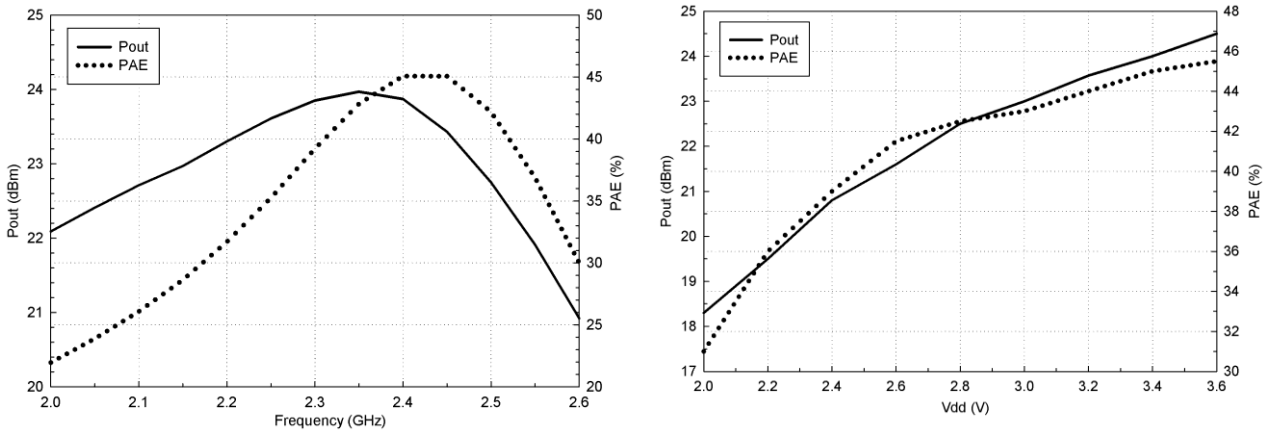


Fig. 6: Output power and PAE vs. input power.

Table 1 shows the comparison of performances of the previously reported switching class E PA and this work. It can be seen that the implementation of bondwires have significant effect on the chip size while other performances such as output power and efficiency are comparable with the previous works. The results from this proposed design also take into account the effect of bonding wires during simulation.



(a) (b)

Fig. 7: Output power and PAE vs. (a) frequency and (b) supply voltage.

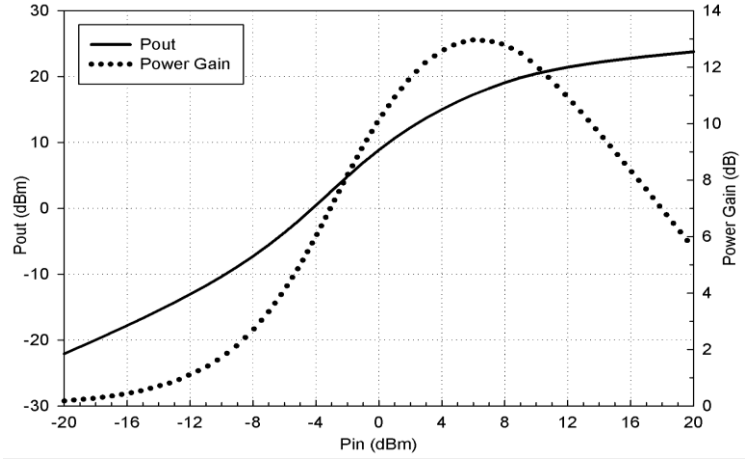


Fig. 8: Output power and power gain vs. input power.

Table 1: Performance summary of CMOS single-ended PAs.

Reference	(Jhin-Fang Huang et. al., 2006)	(Hafez Fouad et. al., 2009)	(Meshkin, R et. al., 2010)	(Yonghoon Song et. al, 2010)	(Zhisheng Li et. al, 2012)	(Yamashita, Y. et. al, 2013)	This work
Technology	0.25µm	0.13µm	0.18µm	0.13µm	0.18µm	0.18µm	0.13µm
Frequency (GHz)	2.4	2.4	2.4	2.4	2.45	5.0	2.4
Vdd (V)	3.3	7	1.8	1.8	2.0	2.0	3.3
Pout (dBm)	24.1	25.8	21.09	31.5	20	15.4	23
PAE (%)	50.6	38.8	58	51	43.6	40.6	45.5
Total Chip Size (mm²)	1.01	N/A	N/A	1.00	2.24	0.81	0.37

Conclusion:

In this paper, a theory of realizing bondwire inductors with CMOS switching class E PA was described. A 2.4 GHz switching class E PA with bondwires inductor for wireless applications has been designed in the 0.13-µm CMOS process. All circuit components, except the output matching network have been designed on-chip and all inductances are realized using bonding wires. The advantage of proposed switching class E PA is promising to reduce the chip size. The post-layout simulation results show that the power amplifier can deliver an output power of 23 dBm with a PAE of 44.5% at 2.4 GHz.

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