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Design A Buck Boost Controller Analysis For Non-Idealization Effects

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ABSTRACT

This paper addressed the design of a buck boost converter based on given specifications by taken into account the non-Idealization of all components, switching device and diode for real application purpose. Depending on the application and power levels, the enclosure of these freeloading effects of both components and devices is very important to design the converter for acceptable performance. The initial stage of the design is based on the basic theoretical calculations. Simulation work has been carried out by Pspice program to validate the operation of the buck boost converter circuit. The performance analysis which covers the non-Idealization effects on related waveforms of output voltage, current and power are discussed and achieved.

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INTRODUCTION

DC-DC converters in power electronic systems are the circuits that convert the system voltages from one DC level to another DC level, often providing a regulated output DC voltage. The converters are employed in a variety of applications for the power ranging from watts (computer power supply, mobile phones), kilowatts (dc motor drives) to megawatts (traction vehicles). There are two frequently used terms for types of DC-DC converters which are non-isolated and isolated. A non-isolated DC-DC converter has a dc path between its input and output. In contrast, an isolated DC-DC converter uses a transformer to eliminate the DC path between its input and output. It is also known that there are three basic topologies commonly use in both types of converters namely as buck, boost and buck boost. These converters also have two different mode of operation either continuous conduction mode or discontinuous conduction mode (Boumediène, A *et al.*, 2013).

Most modeling's in power electronics are mainly planned to convert this non-linear time-varying problem to an easier form. However they are insufficient for some delicate problems since they are based on ideal switches (Rd.middlebrook. Slobodan cuk, 1976). The DC-DC converters can be used to interface the elements in the electric power train by boosting or chopping the voltage levels (Rashid, M.H., 2007), but their use is limited due to the size, weight, efficiency, and cost of current boost DC-DC converter. Recent applications in the design of power supply employ boost DC-DC converters because the required output is inverted directly from the input voltage, and the output voltage can be either higher or lower than the input voltage (Turk *et al.* 2004). The boost power converters are widely used in applications like automotive and marine (Wanes, J., 2004).

A general conventional buck-boost DC/DC converter uses an inverting chopper or a combination chopper, which consists of a buck chopper and a boost chopper (Turk *et al.* 2004; Zhang, Q. and Y. Yin, 2003). The inverting chopper stores output energy in storage device, such as reactor or capacitors. Therefore, the converter efficiency is decreased since the power loss occurs in the storage devices. On the other hands, because the combination chopper has two stages for conversion process, the converter efficiency decreases. Many circuit topologies of DC/DC converters have been studied in order to obtain high efficiency (Qun Zhao. Fred C. Lee, 2003; Xinke Wu. Wei Lu. Turk *et al.*, 2006). finally, the simulation of a non-isolated buck boost converter operates in continuous conduction mode (CCM) is designed and its performance in terms of output voltage, current and output power are evaluated. Nevertheless, the effects of non-idealities due to components (switching device and diode) are observed.

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Circuit Of Non-Ideal Buck Boost Converter:

The general buck boost converter circuit diagram shown in Figure (1). And the equivalent circuit with non ideal components of BUCK BOOST converter is shown in Figure (2).

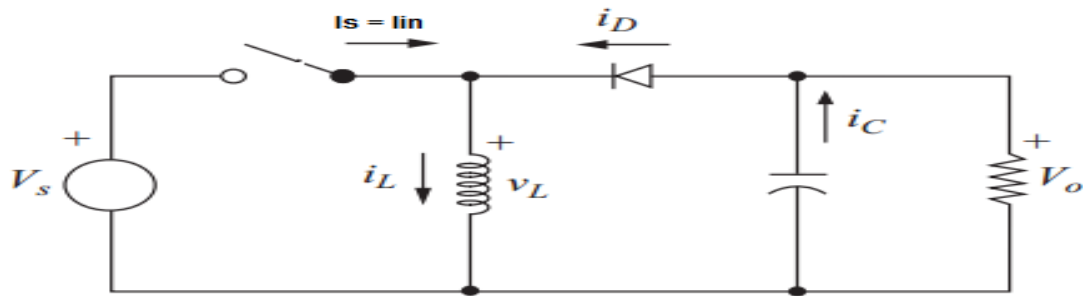


Fig. 1: General buck boost converter circuit diagram.

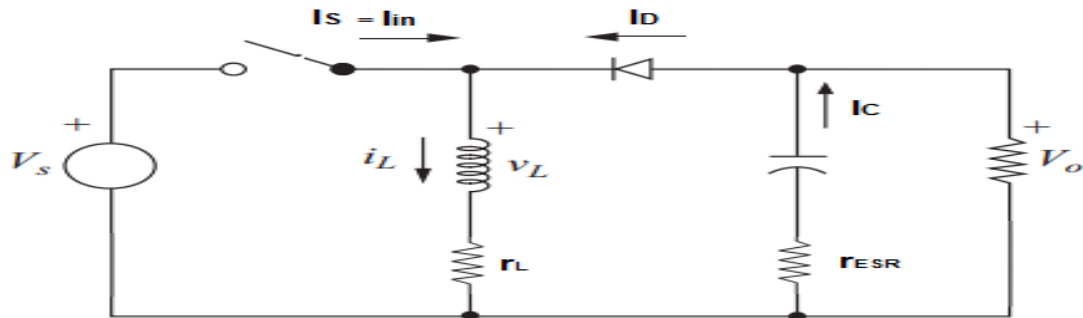


Fig. 2: Buck boost converter circuit diagram (With r_L and r_{ESR}).

The initial approach for the design at the first stage is based on theoretical calculations that consider the effects of V_Q , V_D and $r_{DS(ON)}$ to estimate the circuit parameter values as referred to the basic buck boost converter circuit diagram as shown in Fig. (1). All variables as well as selection of components are described in details in next part. Then, simulation works are carried out by using Pspice simulator to validate the operation and performance of the buck boost converter circuit. Performance analysis due to important key waveforms such as voltage, current and power are evaluated by taken into account for all non-ideal components used in the buck boost converter circuit.

Design Calculations And Considerations:

The steady state operations of the buck boost converter in continuous conduction mode via typical principal waveforms as per theory was done. Switching frequency is set to be 112 kHz. The circuit parameter values are estimated as follows:-

- Load Resistor,

$$R = \frac{V_o^2}{P_o} \quad (1)$$

$$I_o = \frac{P_o}{V_o} \quad (2)$$

-Duty ratio , D

As referred to reference direction in Figure (1), by applying KCL

$$i_{in} = I_o \frac{D}{(1-D)} \quad (3)$$

However, the voltages do not satisfy the simple relationship like (3) due to the voltage across MOSFET via $r_{DS(ON)}$ and diode. Therefore, more precise derivation is needed to calculate the duty-cycle value based on above particular factors. These known mentioned parameters can be obtained from datasheet of MOSFET and diode.

The voltage across the inductor when the switch is ON;

$$V_L = V_{in} - r_{DS(ON)} \cdot I_L \quad (4)$$

The voltage across the inductor when the switch is OFF;

$$V_L = -V_D - V_O \quad (5)$$

Since the average steady-state voltage across an inductor is zero, the equation becomes,

$$D(V_{in} - r_{DS(ON)} \cdot I_L) = (1-D)(V_D + V_O) \quad (6)$$

By rearranging the equations gives the following

$$D(V_{in} - r_{DS(ON)} \cdot \left[\frac{I_O}{(1-D)} \right]) = (1-D)(V_D + V_O) \quad (7)$$

Notes that by choosing small value for $r_{DS(ON)}$ and V_D , and use the specifics values and reorganizing (7) gives the quadratic equation. Thus, $D = 1$ and $D = 0.674$. Since $D = 1$ is not possible to be set as duty cycle value, $D = 0.674$ is chosen. Besides, the value of D can be obtained from the basic buck boost expression.

$$V_{in} = -V_O \frac{D}{(1-D)} \quad (8)$$

- Inductor, L

$$L_{min} = R \frac{(1-D)^2}{2f} \quad (9)$$

$$I_L = \frac{V_{in} D}{R(1-D)^2} \quad (10)$$

The estimation value of L should be larger than L_{min} for the converter to operate in continuous conduction mode.

$$I_{Lmax} = I_L + \frac{\Delta I_L}{2} \quad (11)$$

$$I_{Lmin} = I_L - \frac{\Delta I_L}{2} \quad (12)$$

The inductor current ripple,

$$\Delta I_L = \frac{V_{in} D^2}{fL} \quad (13)$$

As a result, inductance value obtained from (13) is $L = 21.35\mu H \approx 20\mu H$. This approximate value is chosen because of based on inductor datasheet.

-Capacitor, C

The output voltage ripple is set to be 0.2% to estimate the value of C . The govern equation without r_{ESR} is given by

$$\frac{\Delta V}{V} = \frac{D}{RCf} \quad (14)$$

The capacitance value obtained from (14) was $C = 120\mu F$ and because it has small r_{ESR} to satisfied the requirement of the output voltage ripple. This voltage ripple will differ due to the value of r_{ESR} . The govern equation by taken into account the r_{ESR} effect for the buck boost converter circuit is as follows

$$\frac{\Delta V_{ESR}}{V_O} = \left[\frac{1}{R(1-D)} + \frac{(1-D)}{2fL} \right] * r_{ESR} \quad (15)$$

-Selection of power MOSFET and diode

The search for the suitable power MOSFET for a specific application will consider in minimizing the losses and understanding on how losses are dependent on the switching frequency, current, duty cycle and the switching rise and fall times. The MOSFET selection and its intrinsic parameters are based on high breakdown voltage, V_{dss} and current carrying capability, I_d with the lowest on resistance $r_{DS(ON)}$. Lowering the value of $r_{DS(ON)}$, will lower the power dissipated across the power MOSFET for a given RMS current, I_L . It is noted that the choice of power MOSFET to be chosen is due to switch stress on the buck boost converter circuit.

$$\text{Peak voltage stress on the switch : } V_{\text{switch max}} = V_{\text{in}} + V_o \quad (16)$$

$$\text{Peak current through the switch : } I_{\text{switch max}} = I_{L\text{max}} - I_o \quad (17)$$

Based on above switch stress calculation, power MOSFET IRF150 with small gate charge and low $r_{\text{DS(ON)}}$ is selected for the switch.

Diode selection depends strongly upon reverse breakdown voltage, V_{rr} , forward voltage drop, V_f and forward current, I_{ff} or high frequency application. Diode in the buck boost converter plays significant roles during switch OFF time at the output side. Since the voltage and current across the diode that represented by output voltage and current are not too high, diode type BYT30P-400 is chosen since the ratings is sufficient to withstand the highest amount voltage and current in the circuit.

The Pspice schematic diagram of buck boost converter circuit for all known parameters by considers non-ideal elements is shown in Figure (3).

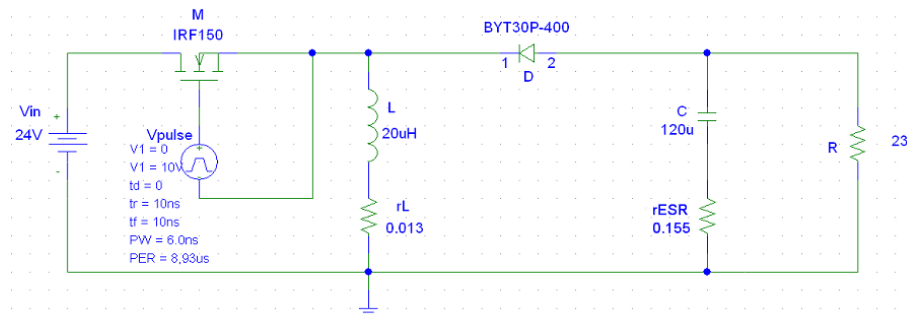


Fig. 3: Pspice schematic diagram of buck boost converter (With r_L and r_{ESR}).

Simulation Results And Discussion:

The simulation analyses are categorized in two main parts which are the observations on particular waveforms for both ideal and non-ideal buck boost converter circuits. The performance analysis on the output voltage and efficiency are evaluated respectively. Whilst, the effects of non-idealization by varying values of r_L and r_{ESR} are also been investigated.

- Analysis On The Buck Boost Converter Circuit (ideal):

a) Voltage and Current at power MOSFET, diode and inductor

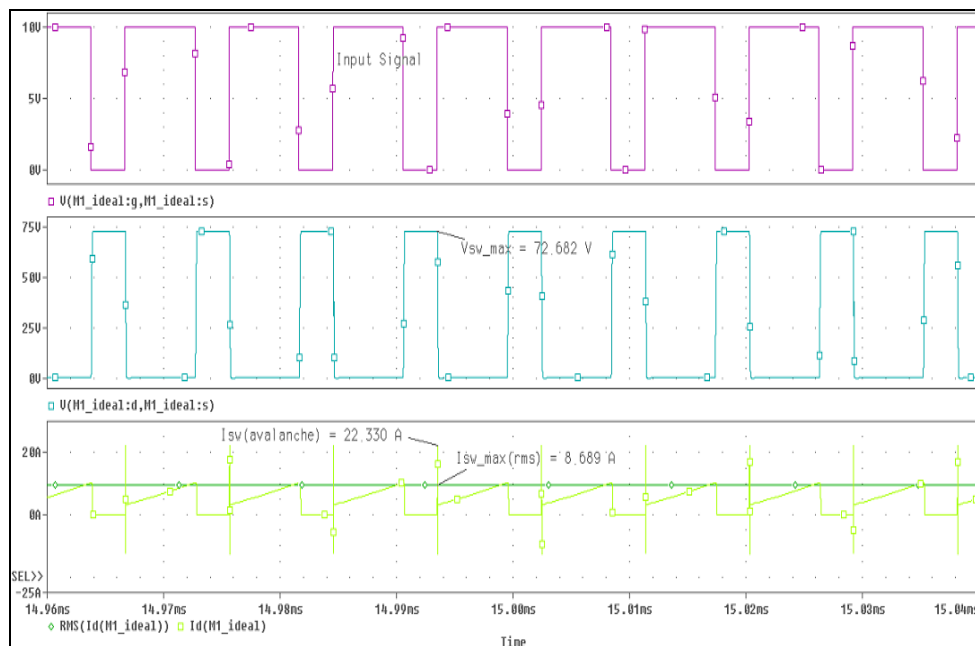


Fig. 4:Power MOSFET voltage and current

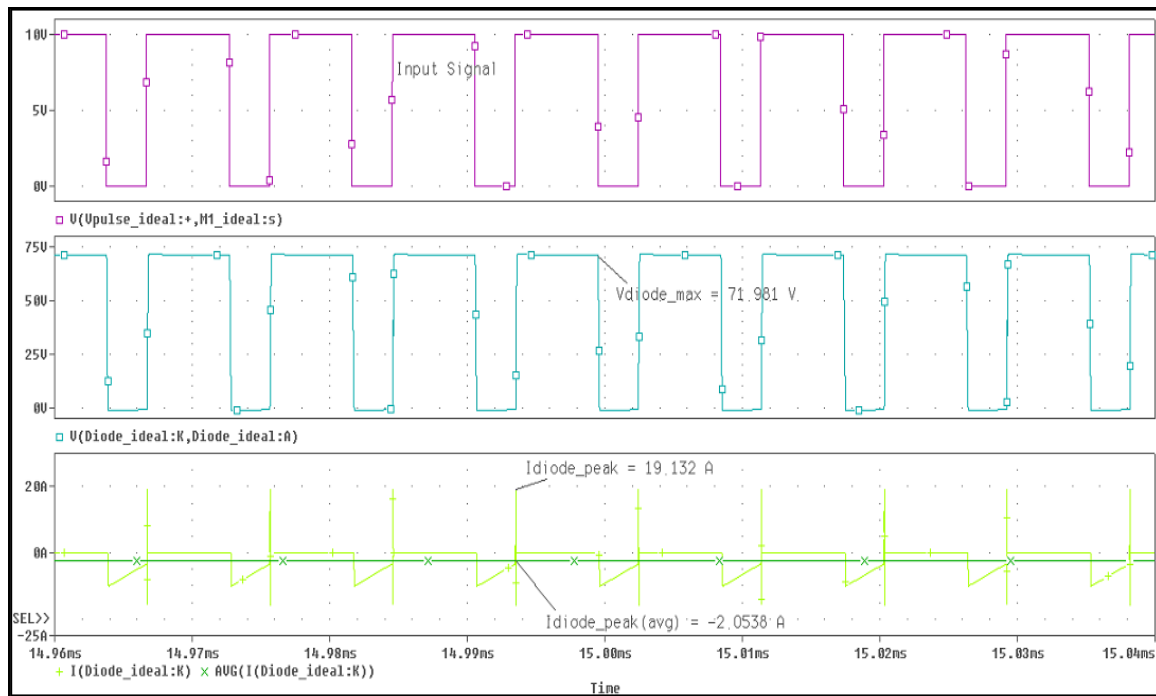


Fig. 5: Diode voltage and current (ideal).

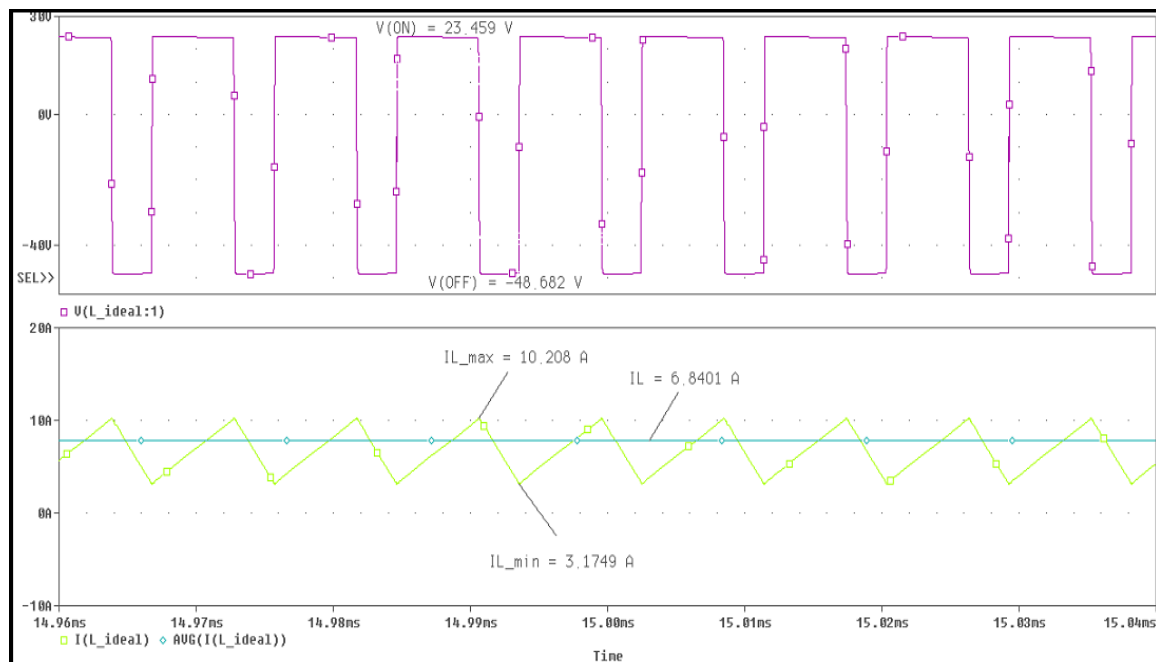
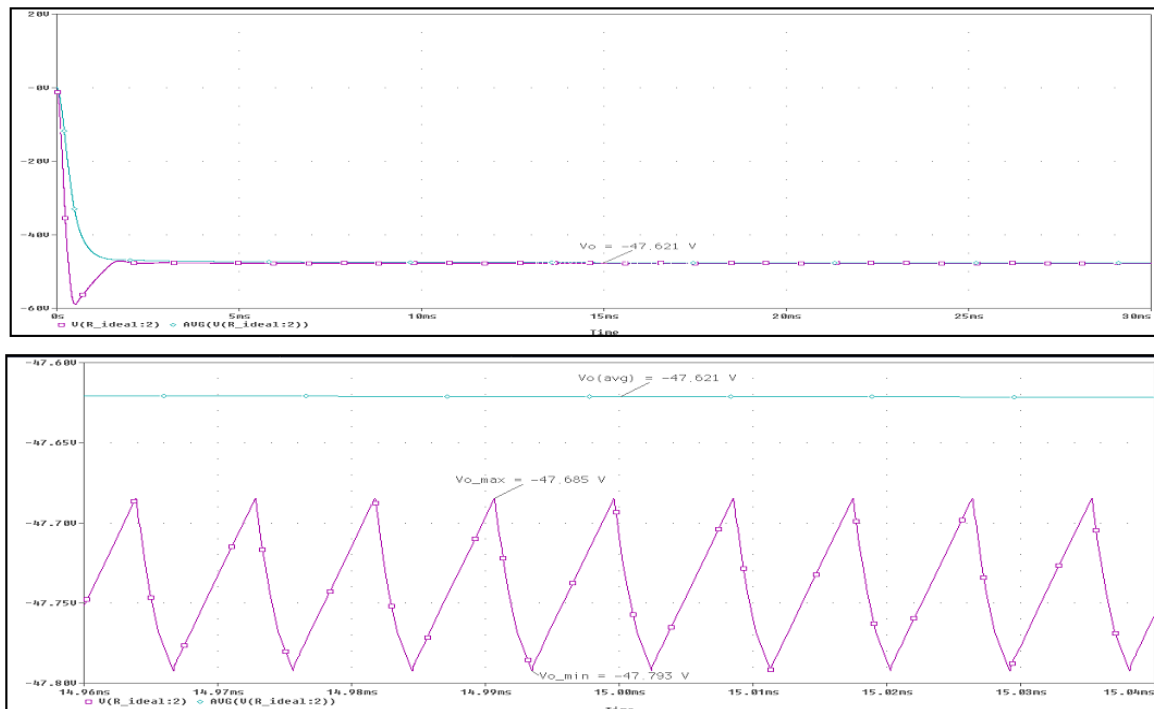
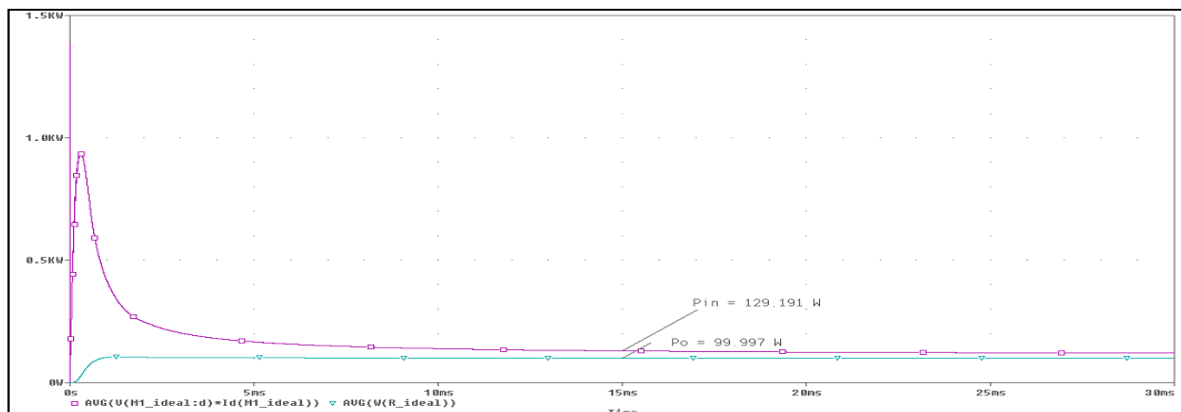


Fig. 6: Inductor voltage and current (ideal)

From Figure (4) and (5) respectively, it can be seen clearly that the peak voltage at the devices as well as the peak current through the devices are in acceptable range for the power MOSFET and diode to operate well in real practical application. All values met the permissible ratings standard as referred to the datasheet. Figure (6) shows the inductor voltage and current. The waveforms proved that the voltage at the inductor during ON state takes the value of V_{in} whilst during OFF state it takes the value of V_o . On the other hand, the current flowing through the inductor represents the mode of operation of buck boost converter that it operates in continuous conduction mode.

b) Output voltage:**Fig.7:** Output voltage (ideal)

The output voltage obtained from the simulation is -47.621 V which is not exact -48 V as illustrated in Figure (7). The ripple curve looks almost triangular for a negligible r_{ESR} . This output voltage slightly drop because of the parasitic elements with regards to voltage drop at the MOSFET, diode and $r_{ds(on)}$ in the switch. Pspice simulation has already taken into account those parameters which can't be visualized at the waveforms. However, the above mentioned parameters are important to be taken into consideration for which they are also contributing into the losses distributions in the circuit. Therefore, it is important to select components with low voltage drop at MOSFET and diode as well as low $r_{ds(on)}$ in perhaps to have low power dissipation in the systems.

**Fig. 8:** Output power (ideal)**- Analysis On The Buck Boost Converter Circuit (non-ideal).****a) Voltage and Current at power MOSFET, diode and inductor**

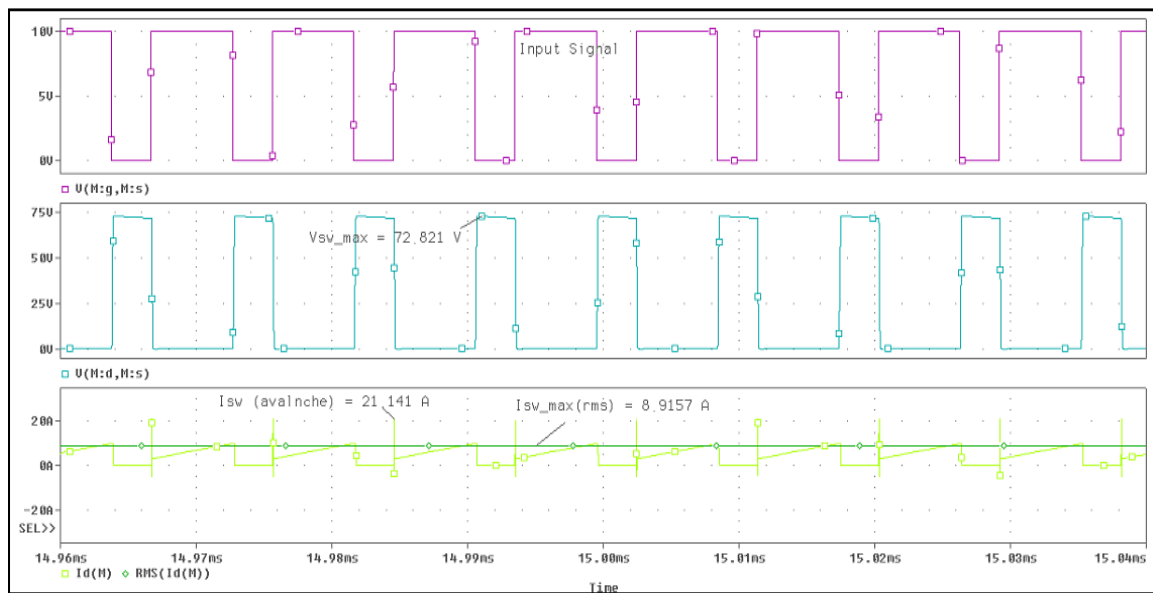


Fig. 9: Power MOSFET voltage and current (non-ideal).

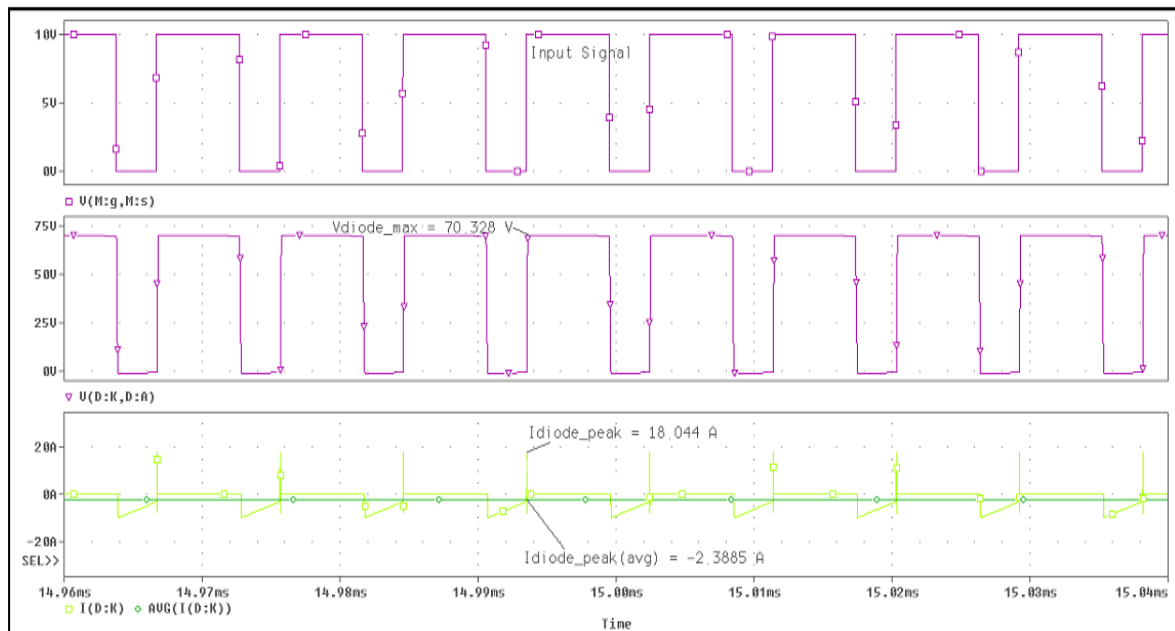


Fig. 10: Diode voltage and current (non-ideal)

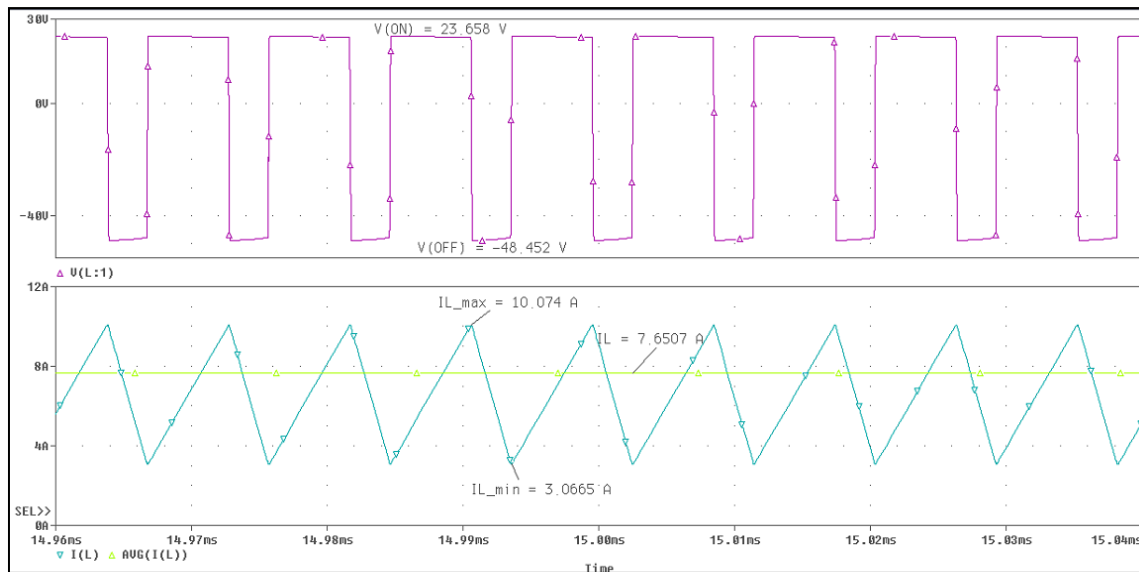


Fig. 11: Inductor voltage and current (non-ideal).

The results obtained in consider the non- Idealization for voltage and current at the power MOSFET. All peak values of voltage and current at the MOSFET and diode as depicted in Figure (9) and (10). The circuit is still operates in continuous conduction mode. The voltage at the inductor increased as compared with results from figure (6) because of adding r_L in series with the inductor. This is because of the presence of r_L has affected values of current flowing through the inductor which mean that the current increased as compared with previous ideal results.

b) Output voltage:

The output voltage obtained from the simulation as shown in Figure (12). The waveform tends to transform into a square wave with repetitive spike in its voltage. This critical phenomenon is because of a combination of capacitor C with the r_{ESR} appeared in series in the circuit. It is observed that the ripple now is no longer across C alone but have also to consider the presence of r_{ESR} .

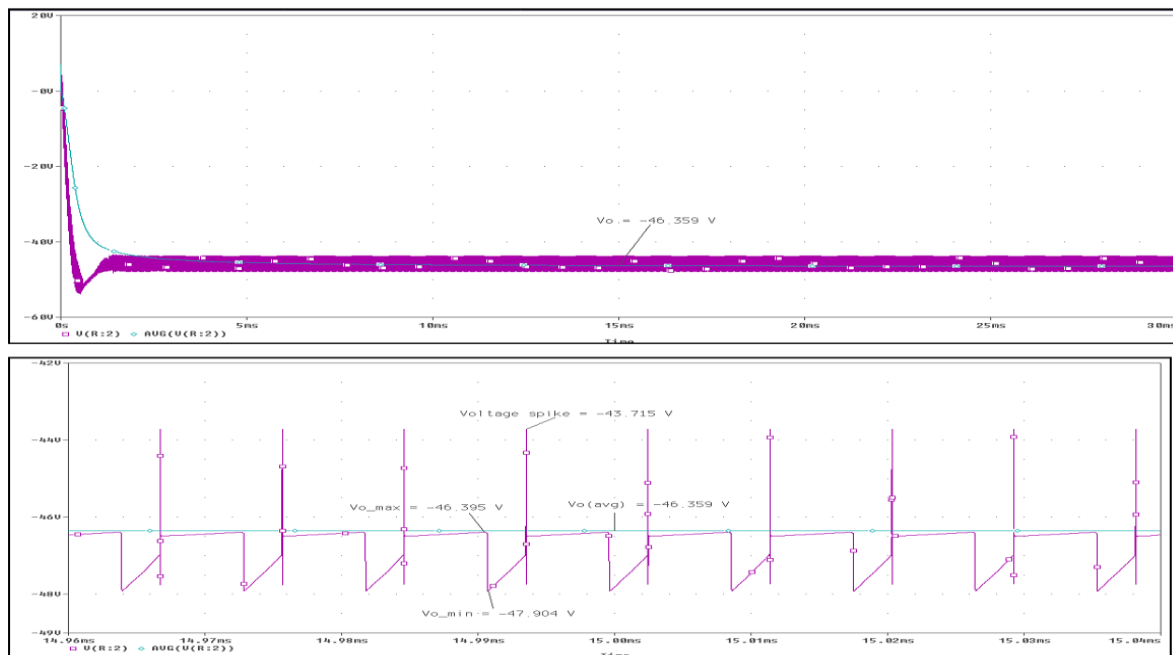


Fig. 12: Output voltage (non-ideal).

c) Power And Efficiency:

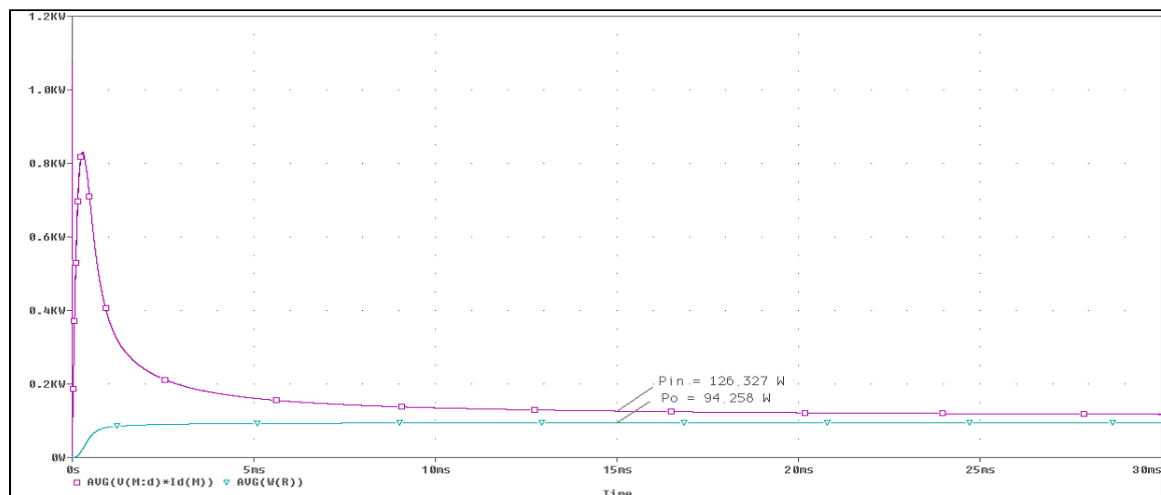


Fig. 13: Output power (non-ideal).

As refer to Figure (13), It can be observed that there are significant power losses in the circuit that contributes into this less output power. This is due to additional resistive elements of r_L and r_{ESR} adding in the circuit (in practical application, r_L and r_{ESR} cannot be seen by naked eyes because they are parasitic elements in inductor and capacitor itself). Besides power losses at the switch and diode, power dissipation at the resistor plays significant effects on the output power. Hence, the efficiency will drop as well.

d) The Effects Of Non- Idealization By Varying R_L And R_{esr} Values:

The simulation works are continued by varying values of r_L (fixed r_{ESR}) and r_{ESR} (fixed r_L). The effects on the output voltage and output power for both conditions are observed in the following waveforms of Figure (14) and (15) respectively:-

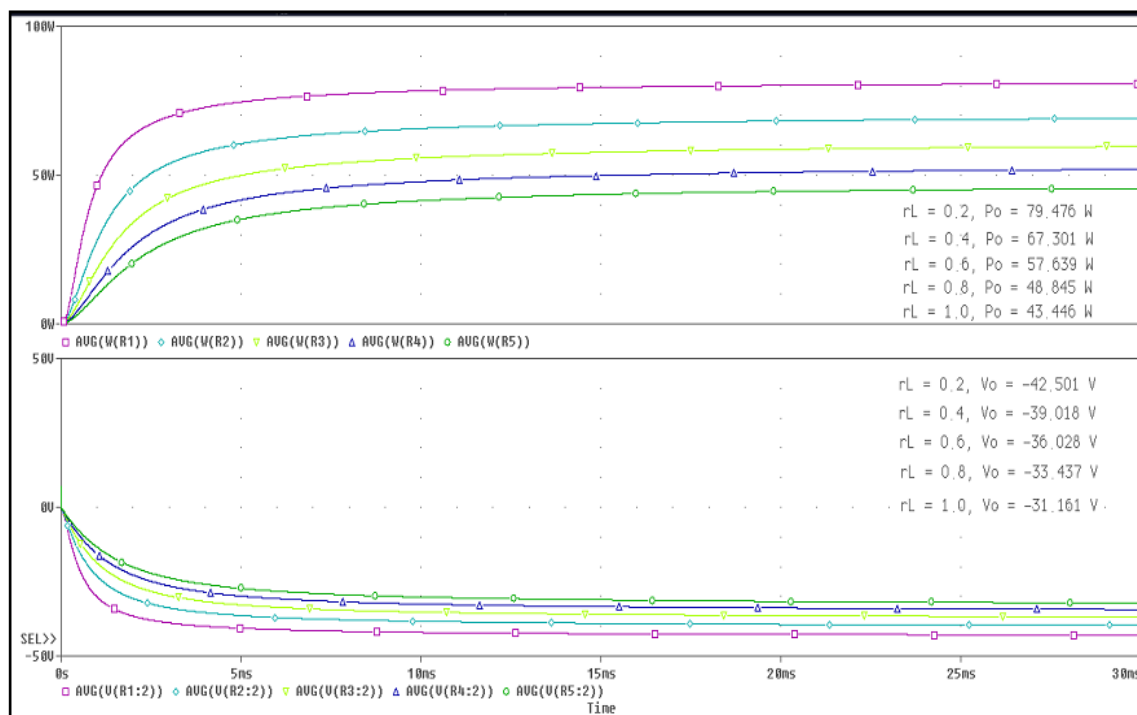


Fig. 14: Output voltage and output power (r_L varied with fixed r_{ESR})

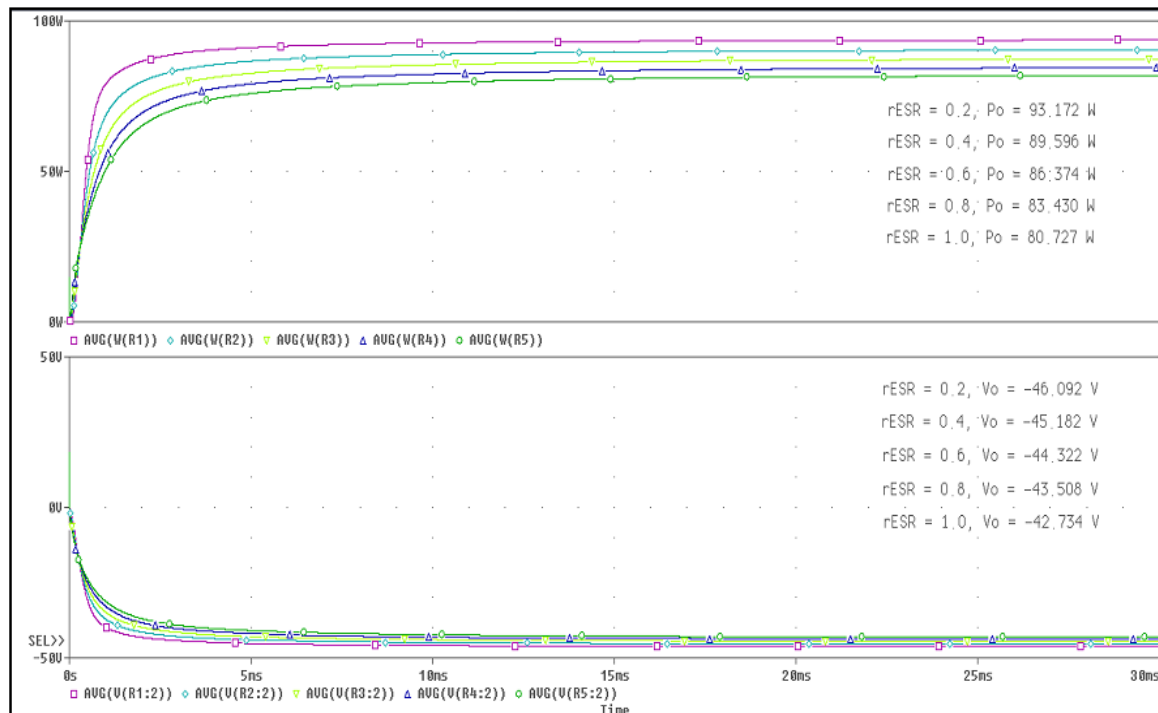


Fig. 15: Output voltage and output power (r_{ESR} varied with fixed r_L).

The Effects of non- Idealization by Varying R_L and R_{ESR} Values can be summarized that the output voltage and power dropped by significant amounts as the values of r_L and r_{ESR} become higher. The output ripple also increased whilst the efficiency are decreased for the higher values of r_L and r_{ESR} .

Design Verifications And Discussions:

The performance evaluations for design verification of the buck boost converter circuit (non-ideal) are achieved. And this converter accomplished to obtain 3% of output ripple voltage even though there are slightly less differ around 4% and 6 % in its output voltage and output power respectively as compared to the objective specifications. The results from the extension simulation works by varying values of r_L and r_{ESR} has proved that as the values of r_L and r_{ESR} increase, the output ripple voltage increased whilst the output voltage and output power decreased significantly.

Conclusions:

This paper proposed a design of buck boost converter with specification data, and focused on the output ripple voltage instead of output power. Although the requirement of output power is not satisfied but the ripple voltage is confirmed for design validation. It is known that the design constraints are also limited to the values of elements used in the circuit as well as the selection of the components. Therefore, the intrinsic elements presence in the components such as $r_{DS(on)}$, r_L , r_{ESR} and etc are very important to be known which all these parameters would affect the performance of the converter. In this paper give a appropriate technical and simulation approaches with lots of analysis to get best optimum design of the buck boost DC-DC converter circuit.

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