Design of low power high speed (LPHS) SRAM cell for write operation

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ABSTRACT

Background: Modern technology is spreading with a very fast rate and time to market is very less, the parameter which is greatest today becomes worst tomorrow. A key in improving the performance of the system is to use an optimum sized SRAM. Cell stability and low power static random access memory (SRAM) are the main concerns and has become a critical component in modern VLSI systems. To establish larger reliability and longer battery life for portable application, low power SRAM array is necessity. Objective: The main objective of this research paper is to propose new SRAM architecture to reduce the power consumption because write power consumption in any SRAM cell is a significant portion of the overall power consumption due to large voltage swing in the large bit lines. Results: Due to proposed architecture of the cell, the write power consumption reduces about 77% compared to the 6T cell due to lower discharging activity at bit lines. Conclusion: Due to lower discharging at the bit line, the write access delay reduces compared to the other cells. The read stability also improved in the proposed SRAM cell. The proposed cell can be used in mobile applications where power saving is a critical issue and this cell can even be used in worse temperature condition with minimum power loss.

INTRODUCTION

The power has become an important consideration in the design of VLSI and the microprocessor system as the demand for portable devices and embedded systems continuously increased. The on-chip caches can reduce the speed gap between processor and main memory. These on-chip caches are typically implemented using arrays of densely packed SRAM cells. Through the years, the requirement for power reduction in SRAM has seen tremendous progress (Kanak Agrawal et al., 2008, Azeez J. Bhavnagarwala et al., 2008, Rajiv V. Joshi et al., 2009 and Vinod Ramadurai et al., 2009). SRAM cells includes read and write operation. The write power is usually higher than the read power due to the large power dissipation in driving the cell bit-lines to full swing. The power dissipated in bit-lines represents 70% of the total SRAM power consumption during a write operation. Many techniques have been proposed to reduce the write power consumption by reducing the voltage swing level on the bit-lines (Yen-Jen Chang et al., 2004, Kanda, K et al., 2004, Aly, R.E. et al., 2007, Prabhu, C.M.R et al., 2009 and Prabhu, C.M.R et al., 2010). The proposed ZA (Yen-Jen Chang et al., 2004) as well as low power 7T (Aly, R.E. et al., 2007) SRAM cells are designed for power reduction in write ‘0’ operation.

In this paper, we have mainly concentrate on power saving and lower access delay during write “0” as well as write “1” operations. The LPHS SRAM cell is proposed to reduce the activity factor of the discharging of the bit line pair during write operation. All the results were obtained in 0.12μm CMOS technology using Microwind3 CAD tools (Etienne Sicard, 2005). We evaluate the following characteristics for SRAM cell using the proposed SRAM cell: power consumption, area, write/read access time and static noise margin. The rest of the paper is organized as follows. The proposed LPHS SRAM cell is explained in section II. The simulated results of write power consumption, write/read performance, Static Noise Margin (SNM) are presented in section III. The layout of the LPHS SRAM cell is shown in section IV and section V concludes the paper.

Proposed Circuit Description:

The schematic of the proposed LPHS cell is as shown in Figure 1. The proposed LPHS SRAM cell contains an extra two nMOS transistors N5/N6 which are connected in between two inverters, inv1 and inv2. The switching behavior of these two bridging transistors is controlled by the logic levels at write signals (W1 and...
The write operation of this proposed cell depends on the detaching the feedback link between two inverters and disconnecting the bit line (BL and BLB) by using two write access transistors (N3 and N4). The two write access transistors are controlled by word line signals (WL1 and WL2).

Fig. 1: LPHS SRAM cell

The write operation of the proposed LPHS SRAM cell depends on cutting off the feedback connection of the inverters using two bridging transistors (N5 and N6). N3/N4 is turned ON while N4/N3 is turned OFF, BLB/BL carries complement of the input data. The write operation in the proposed SRAM cell is performed by setting the bit lines (BL and BLB) to the desired logic and enabling the access transistors N4/N3. To write ‘0’ at node Q the bit line has to be set at BLB = 1. BL (bit line bar) carries complement of the input data; transistors N6 is turnover while transistors N6 and N4 are turned OFF before asserting WL1 to high. Once WL1 is high, the access transistor N3 is turned ON by WL1 and the access transistor N4 is turned OFF by WL2. BL is disconnected from the node Q1 as shown in Fig 2(a). This LPHS cell forms two cascaded inverters, inv.1 followed by inv.2, as shown in Fig. 2(b). N3 transistor transfers the data from BLB to Q2 which drives inv.2, P2 and N2, to develop Q which equals Q1. Then, both bit lines (BL and BLB) are precharged while transistor N5 is turned ON to reconnect the feedback link between the two inverters. Due to the reconnection of the feedback link, the proposed cell is stably store the new data.

Fig. 2: (a)LPHS during write ‘0’ operation  
(b) Equivalent circuit

Fig. 3: (a)LPHS during write ‘1’ operation  
(b) Equivalent circuit

To write ‘1’ at node Q the bit line has to be set at BL = 1. BLB (bit line bar) carries complement of the input data; transistors N5 is turn ON, while transistors N5 and N3 are turned OFF. Once WL2 is high, the access transistor N3 is turned OFF by WL1. Therefore, BLB is disconnected from the node Q2 as shown in Fig. 3(a).
This LPHS cell forms two cascaded inverters, inv.2 followed by inv.1, as shown in Fig. 3(b). N4 transistor transfers the data from BLB to Q2 which drives inv.1, P1 and N1, to develop QB which equals Q2. Then, both bit lines (BL and BLB) are precharged while transistor N6 is turned ON to reconnect the feedback link between the two inverters. Due to this feedback mechanism, the proposed LPHS SRAM cell consumes lower power and faster response compared to the conventional 6T SRAM cell during write operation.

During read operation, both BL and BLB are precharged to VDD and World lines (WL1 and WL2) are always selected to high, so that the proposed LPHS SRAM cell behaves like conventional 6T SRAM cell. When Q=“0”, the read path consist of N2, N4, and N6, as shown in the fig. 4(a). When Q=“1”, the read path consist of N1, N3, and N5. In both critical cases, the three series connected transistors diminish the driving capability of the cell unless these transistors are carefully sized.

![Fig. 4: Critical path](image)

### RESULTS AND DISCUSSIONS

This section provides the detailed simulation analysis of the LPHS SRAM cell with help of BSIM4 based transistor model for 0.12µm logic process technology, and VDD=1.2V. Threshold voltage of nMOS (pMOS) is set to 400mV. We first estimate impact of the proposed SRAM cell on the power consumption and performance that includes read and write access time. The write simulations are performed for power consumption and write access time.

Since in the conventional 6T cell, one of the two bit lines must be discharged to low regardless of written value, therefore the power consumption in both writing ‘0’ and ‘1’ are the same. In contrast, the 7-T cell (Aly, R.E et al., 2007) uses the complement of input data to perform the write operation that prevents the single write bit line from being discharged if the written value is ‘0’. Therefore, the write ‘0’ power is far less than the write ‘1’ power in the 7-T cell (Aly, R.E et al., 2007). In our proposed LPHS SRAM cell, we are preventing any single bit line from being discharged during write 0 as well as write ‘1’ mode by selecting the word lines (WL1 and WL2) to the desired logic which turned either N3 and N4 OFF. The simulated results of power consumption in all the three SRAM cells, for 0→0, 0→1, 1→0 and 1→1 write operations are given in Table I. Due to cutting-off one of the feedback connection, 75% (75%) write power reduction can be achieved in the 0→0 (1→1) write pattern. Compared to the conventional cell, in the 0→1 (1→0) write pattern, a cell reduces the power consumption by 77.59% (77.69%). From results, it is clear that the proposed LPHS SRAM cell consumes 76.32% less power than the conventional SRAM cell. This power reduction is due to introduction of an extra two nMOS transistors N5/N6 which are connected in between two inverters, inv.1 and inv.2. The read power consumption is increased by 9% than the conventional read power due to the increase in the cell size which leads to longer word line interconnect and using four separate wires, WL1, WL2, W1 and W2, to activate the cell.

<table>
<thead>
<tr>
<th>WRITE OPERATION</th>
<th>0 → 0</th>
<th>0 → 1</th>
<th>1 → 0</th>
<th>1 → 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power (µW) 6T</td>
<td>0.002</td>
<td>30.699</td>
<td>30.695</td>
<td>0.002</td>
</tr>
<tr>
<td></td>
<td>7T[6]</td>
<td>0.0015</td>
<td>31.672</td>
<td>6.839</td>
</tr>
<tr>
<td>LPHS</td>
<td>0.0005</td>
<td>6.880</td>
<td>6.847</td>
<td>0.0005</td>
</tr>
<tr>
<td>Delay (ps) 6T</td>
<td>-</td>
<td>111</td>
<td>111</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>7T[6]</td>
<td>-</td>
<td>117</td>
<td>62</td>
</tr>
<tr>
<td>LPHS</td>
<td>-</td>
<td>64</td>
<td>64</td>
<td>-</td>
</tr>
</tbody>
</table>

Table I: Write power and write delay
Table II: Read power and read delay

<table>
<thead>
<tr>
<th>READ OPERATION</th>
<th>0 → 1</th>
<th>1 → 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power (µW)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6T</td>
<td>28.497</td>
<td>28.495</td>
</tr>
<tr>
<td>LPHS</td>
<td>31.021</td>
<td>31.015</td>
</tr>
<tr>
<td>Delay (ps)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6T</td>
<td>80</td>
<td>80</td>
</tr>
<tr>
<td>7T[6]</td>
<td>81</td>
<td>90</td>
</tr>
<tr>
<td>LPHS</td>
<td>91</td>
<td>91</td>
</tr>
</tbody>
</table>

Since VLSI circuits often operate at high temperature, we have simulated the SRAM cells varying temperature in the range from 27°C to 137°C for estimation leakage power, because leakage current (subthreshold current) poses a serious threat for applications where there is potential for high temperature. The subthreshold current is controlled by carrier diffusion, therefore leakage power increases exponentially with temperature. In the proposed LPHS SRAM cell, the increase in leakage power is minimal even at 137°C compared to the 6T cell as shown in Fig. 5. This makes the LPHS cell suitable for low power cache design.

Fig. 5: Leakage Power with temperature

Fig. 6: Read Delay

For a write operation, the write delay is defined as the time between the activation 50% of WL to when nQ is 90% of its full swing. The write access time is approximately equals the propagation delay of inv.2 and inv.1. Because inv.1/inv2 is only driving the diffusion capacitor of N5/N6, it is better if its input capacitance reduces as much as possible to reduce the load on inv.2/inv.1. Therefore the 1→0 / 0→1 write transition time of the proposed LPHS cell is lower than the conventional 6T cell (Table I) as seen in Fig. 2.

The read delay is defined as the elapsed time from asserting WL to the sufficient bit-line swing for correct data sensing (Prabhu, C.M.R et al., 2010) and reasonable bit-line swing is 10% of the full supply voltage. The two ON nMOS (N5/N6) transistors in the critical path in the (Fig. 4) degrades the read access time of the LPHS SRAM cell due to an increase BL/BLB discharge time. This loss due in delay can be compensated by enlarging width of the tail transistors to 2.5xL (length of the channel) as seen in Fig.6. Due to an increase in width of tail transistors, the power consumption increases by less than 0.1%. The read operation is similar to the conventional SRAM cell but careful transistor sizing is required to maintain the same read delay in the case of the conventional cell.

In this paper, we have used SNM (static-noise margin) as the metric to characterize the read stability. The SNM is defined as the maximum value of the dc noise voltage that can be tolerated by the SRAM cell without changing the stored bits (Seevinck, E et al., 1987). The SNM can be graphically measured on the butterfly curve. The static voltage transfer characteristics of the 6T cell and LPHS cell during read operation are shown in Fig. 6(a). The read SNM of the proposed 8-T cell is 165mV at Vth=0.4V (before enlarging the width of the tail transistors). In the LPHS SRAM cell, the transistors N1, N5, N2 and N6 should be enlarged to compensate the stability loss due to inclusion of tail transistors in the LPHS cell. The proposed cell has the SNM of 325mV.
(after choosing ratio of W/L of two tail transistors equal to 2.5) which is approximately x1.7 higher than the 6T cell (195mV). Enlarging the transistor width will increase the driving strength which results increase SNM in the proposed LPHS cell. The read SNM of the proposed LPHS cell is 165mV at Vth=0.4V (before enlarging the width of the tail transistors). The read SNM of the LPHS cell improves by approximately 73% as the threshold voltage of the tail transistor increases from 0.3V to 0.7V as shown in Fig.6 (b). Increase in threshold voltage lowers the leakage current which results in improved read SNM.

![Graphical Representation of SNM](image)

**Fig. 6: (a) Graphical Representation of SNM**

![SNM with threshold voltage](image)

**Fig. 6(b): SNM with threshold voltage**

The layouts of the LPHS and 6T SRAM cells, as shown in Fig. 7, are generated by using 0.12µm design rule. The proposed cell uses 2 more transistors, one extra wordline (WL2) and two write select signals (WS1 and WS2) for read and write operations compared to the conventional 6T SRAM cell. Due to an extra wordline and write select (WS) signals, the cost of wire connection in the proposed cell is more than the conventional cell. Compared to the conventional cell (6.5μm²), the LPHS cell is increased 9.25μm² and hence, the effective area overhead is 11.5%. Because, the percentage of cell array to cache area is about 70%, the overall cache overhead is roughly (11.5%×70%) ~8%.

![Layout of the design](image)

**Fig. 7: Layout of the design**
Conclusions:

Most SRAM low power techniques have been developed to reduce the power only in read. Since, in the SRAM cell, the write power is generally higher than the read power. The 7-T SRAM cell is zero consciously designed to reduce only write "0" power. In the proposed LPHS cell, a new write technique is used to reduce the power of write "0" and write "1" operation by introducing two bridging transistors. The proposed LPHS gives lower delay cell during write operation when comparing with the conventional 6T SRAM cell. The dynamic power dissipation in our proposed SRAM cell is compared to be lower than other SRAM cells during the write mode transitions. The main disadvantage of the proposed cell is its area overhead and larger read/write access delay compared to the 6T cell.

REFERENCES


