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Optimum Design of Single Stage Interleaved DC-DC Converter with Reduced Inductor Volume

[1]P. Vinoth Kumar, [2]Dr.Suresh A, [3]Dr.Rashmi M.R

[1]*Research Scholar, Department of Electrical and Electronics Engineering, St. Peter's University, Chennai, 600054, Tamilnadu, India.*
[2]*Professor, Department of Electrical and Electronics Engineering, SA Engineering College, Chennai, 600077, Tamilnadu, India.*
[3]*Associate Professor, Department of Electrical and Electronics Engineering, Amrita Vishwa Vidyapeetham, School of Engineering, Bangalore, 560035, India.*

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ABSTRACT

There is ever growing demand for high voltage DC. Boost converter helps in meeting high DC voltage demands for most of the applications which are utilising low voltage renewable energy sources. As the power demands from these supplies increase, a single power stage may be insufficient. This paper presents an interleaved-boost approach, which provides efficiency, size, and cost advantages which can be extended to multistage. A single stage interleaved converter with minimum inductance volume is proposed. The simulation is carried out using Multisim software and the simulation results are experimentally validated for the proposed design.

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INTRODUCTION

The electrical energy available in the utility grid is not suitable for direct use in many applications. In particular, applications requiring DC voltage/current source must involve an interface device between the AC power line and the load requiring the DC voltage (Jen-Ta Su et al., 2012). Modern AC-DC switch–mode converters involve at least two cascaded stages. The first stage is the AC-DC conversion stage that interfaces the utility grid voltage with a compatible DC voltage level. The second stage is a DC-DC converter stage that conditions the voltage in the first stage such that the performance requirements of the load are satisfied. The input power quality of the AC-DC conversion stage is critical in most of the power converters, in particular for converters involving power ratings surpassing kilowatts. Further, the DC load power quality requirements have also become stringent (Doo-Yong Jun, 2010; Hiroyakikosai, 2011). In many applications constant DC bus voltage is favourable as the load performance can be easier maintained with the fixed bus rather than load dependent DC bus (Pyosoo Kim et al., 2011). Boost converter based power supplies not only help in stepping up the voltage from low voltage sources, but also improves the power factor. As the power demands from these supplies increase, a single power stage may be insufficient, an interleaved-boost approach is better compared to single boost converter in terms compactness, efficiency and economy (II-Oun Lee, 2013; GU Jun-yin, 2010; Pyosoo Kim, 2011; C.N.M. Ho,2011, Hanju Cha, 2011).

In this proposed work the two–phase interleaved boost power factor corrector which is controlled by the average current mode control method is investigated, its computer simulations are performed.

Corresponding Author: P.Vinoth Kumar, Department of Electrical and Electronics Engineering, Research scholar, St.Peter's University,Chennai,600054, Tamilnadu, India.
E-mail: vinothkumarktp@gmail.com

Description of The Proposed Topology:

Figure1 shows the block diagram of the proposed topology. The AC supply voltage is rectified using full bridge rectifier and fed to interleaved Boost converter, the circuit diagram of which is shown in Figure2. The output of interleaved converter feeds the load. The controlled switching pulses are given to the switches in interleaved converter to obtain the required output voltage.

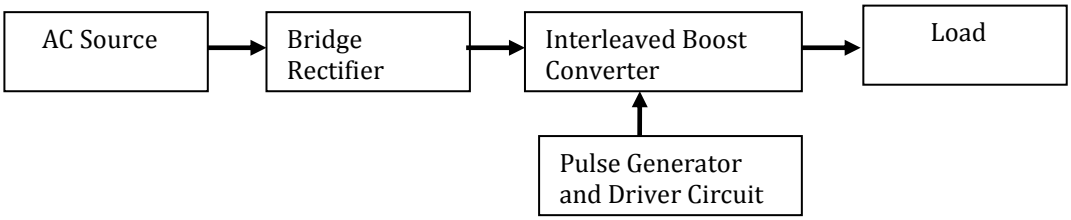

Fig. 1: Block Diagram of the Interleaved Boost Topology

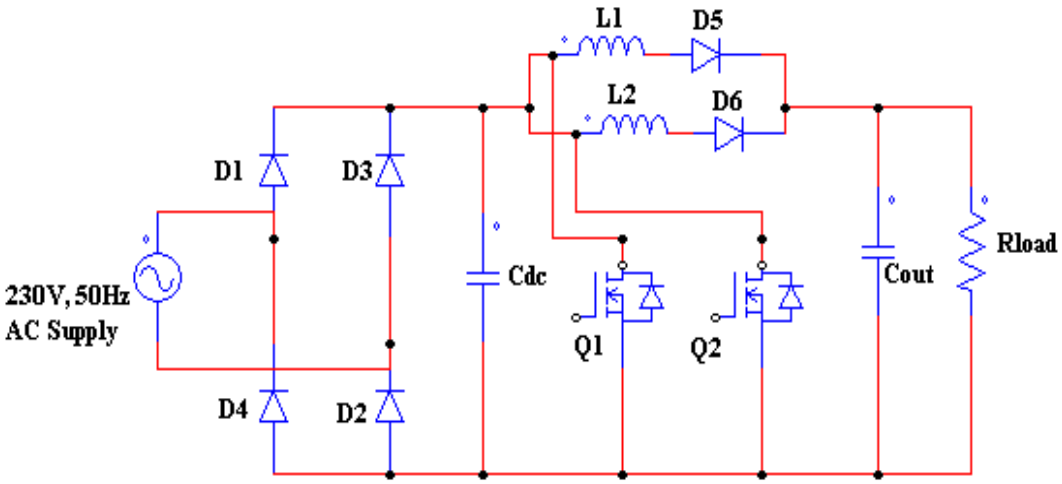

Fig. 2: Circuit Diagram of Interleaved Boost Topology

Design Consideration:

A 400W PFC application with input voltage of 30Vis selected as a design example. The design specifications are as follows: Line voltage range: 30V AC, 50Hz, Nominal output voltage and current: 64V(40W)Output voltage ripple: less than 4Vp-p,

Switching frequency: 10 kHz.

Boost Inductor Design**:**

The boost inductor value is determined by the output power and the minimum switching frequency (C.N.M. Ho *et al*., 2011).

$$f=\frac{1}{T_{ON}}\frac{V_{out}-\sqrt{2}V_{line}}{V_{out}} \quad (04)$$

Where: V_{line} is RMS line voltage; T_{ON} is the MOSFET conduction time; and V_{out} is the output voltage.

The MOSFET conduction time with a given line voltage at a nominal output power is given as:

$$T_{ON}=\frac{2P_{out}}{\eta V^2}L \quad (05)$$

where: η is the efficiency; L is the boost inductance; and P_{OUT} , is the nominal output power per channel,

Therefore, once the output voltage and minimum switching frequency are set, the inductor value is given as (C.N.M. Ho *et al*., 2011):

$$L=\frac{\eta V_{line}^2}{2P_{out}f_{SW}}.\frac{V_{out}-\sqrt{2}V_{line}}{V_{out}} \quad (06)$$

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As the switching frequency decreases, the switching loss is reduced, while the inductor size and line filter size increase. Thus, the switching frequency should be determined by the trade-off between efficiency and the size of magnetic components.

Once the inductance value is decided, the maximum peak inductor current at the nominal output power is obtained as:

$$I_{L_{(peak)}} = \frac{2\sqrt{2}P_{out}}{\eta V_{line}} \quad (07)$$

Output Capacitor Selection

The output voltage ripple should be considered when selecting the output capacitor. Figure 16 shows the twice line frequency ripple on the output voltage. With a given specification of output ripple, the condition for the output capacitor is obtained as:

$$C_{out} = \frac{I_{out}}{2\pi f_{lV_{out(ripple)}}} \quad (08)$$

Where: I_{OUT} is total nominal output current of two boost PFC stage and $V_{OUT,RIPPLE}$ is the peak-to-peak output voltage ripple specification.

Maximum DC Output Current**:**

$$I_{out(max)} = \frac{2P_{max}}{V_{out}} \quad (09)$$

Table 1: Gives different components used in proposed work

PARAMETERS	VALUES
Input Voltage	30V
Inductance(boost)	470uH
Switching Frequency	10KHz
Switching device	FDP18N50 / DPF18N50 500V ,18A
Duty Cycle	0.5
Output Capacitance	440uF
Max Current	0.64A
Output Resistance	100 OHM(5A)
Peak Inductor Current	2.0A
Output voltage	60V

Simulation Result:

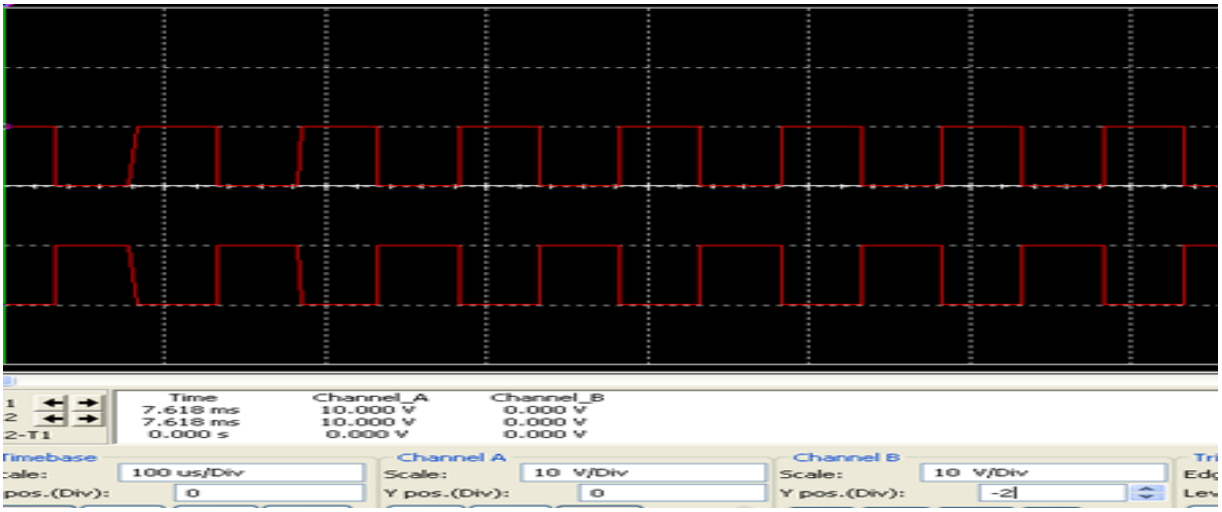

Fig. 6: Output waveform of the triggering circuit.

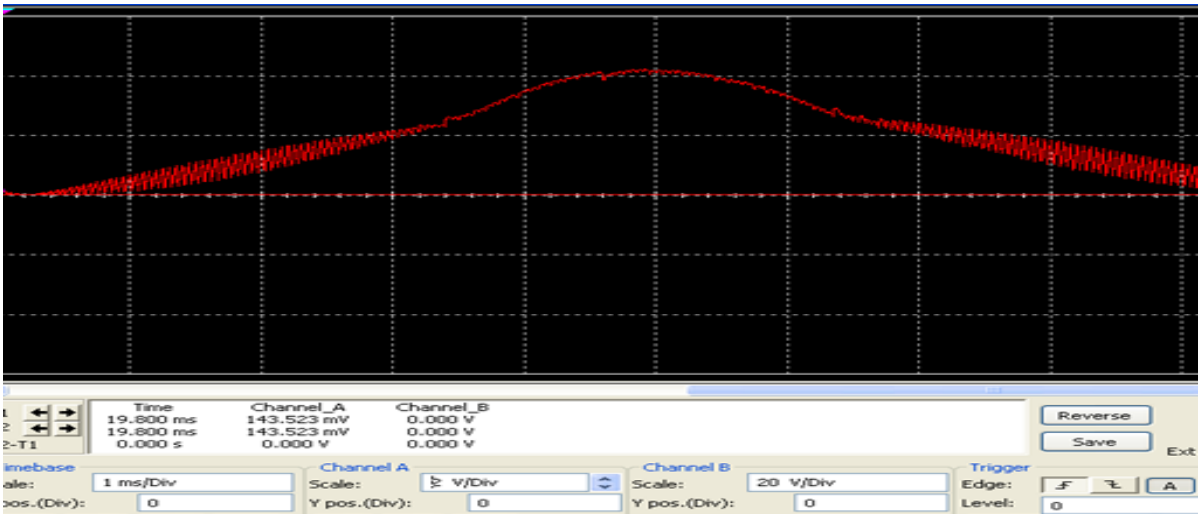

Fig. 7: Input ripple current with interleaving

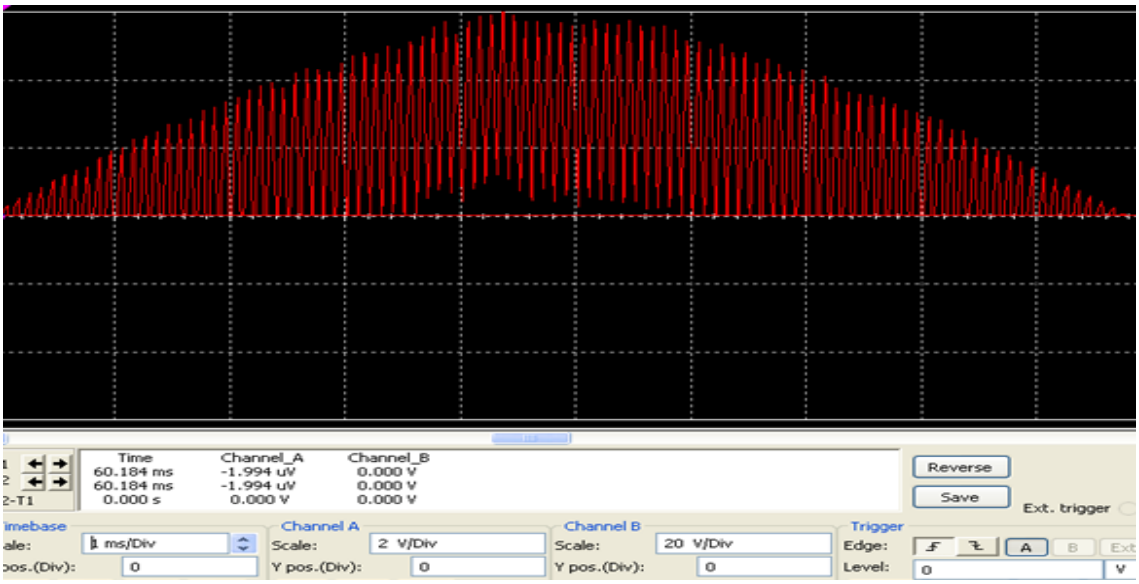

Fig. 8: Input ripple current without interleaving

The magnitude of ripple current is more in circuit without interleaving(figure 8) but very less in circuit with interleaving(figure 7) ,this is due to ripple current cancellation.

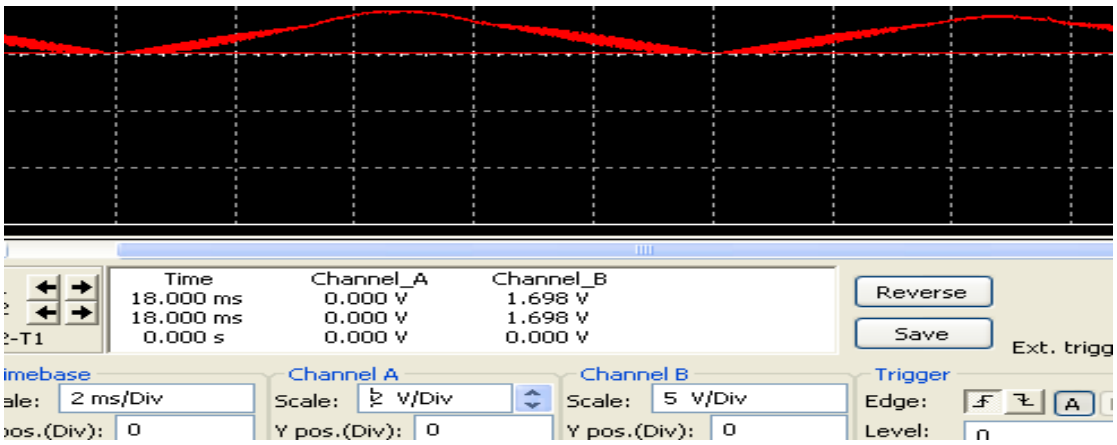

Fig. 9: Diode rectifier output current:

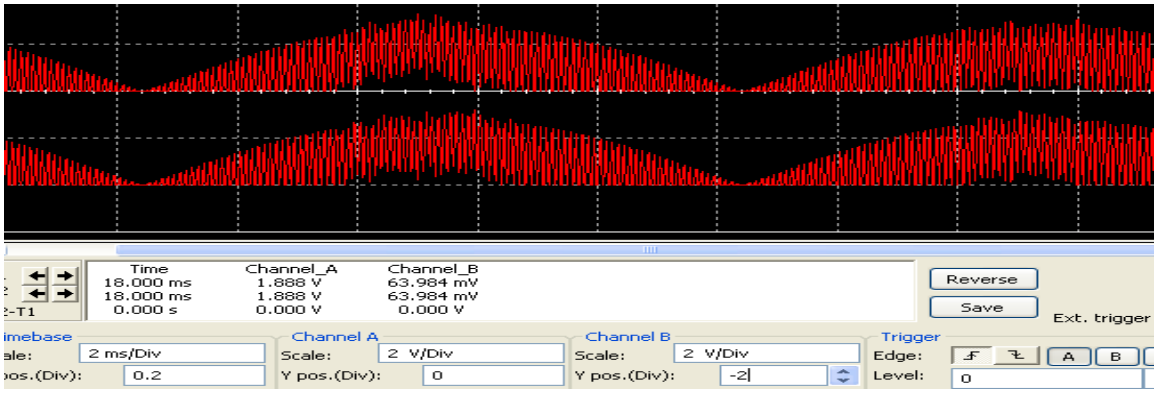

Fig. 10: Inductor currents of the two legs.

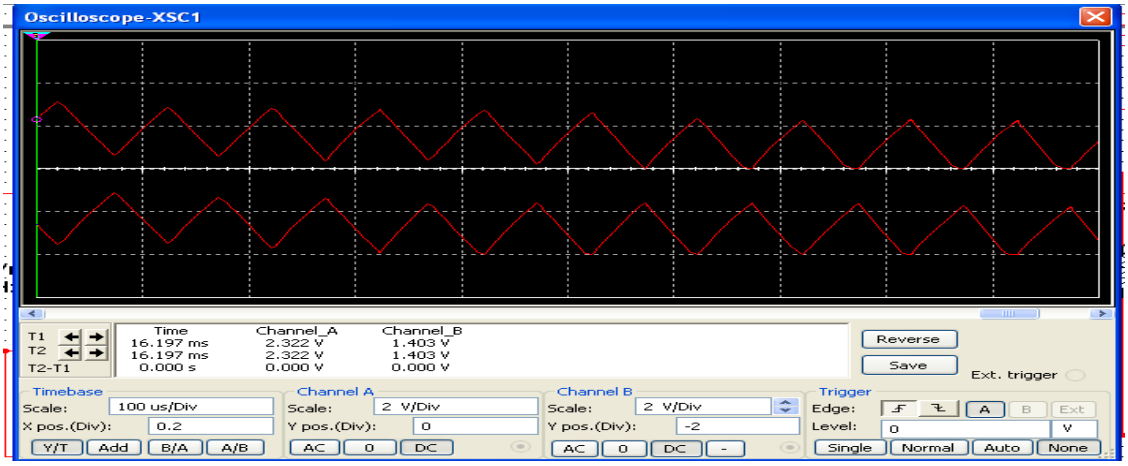

Fig. 11: Inductor currents of two leg showing boundary condition mode

From fig -9 there is reduction in the magnitude of diode rectifier output current, although the current in the individual inductor is high, this is due to the cancellation of inductor currents due to interleaving.

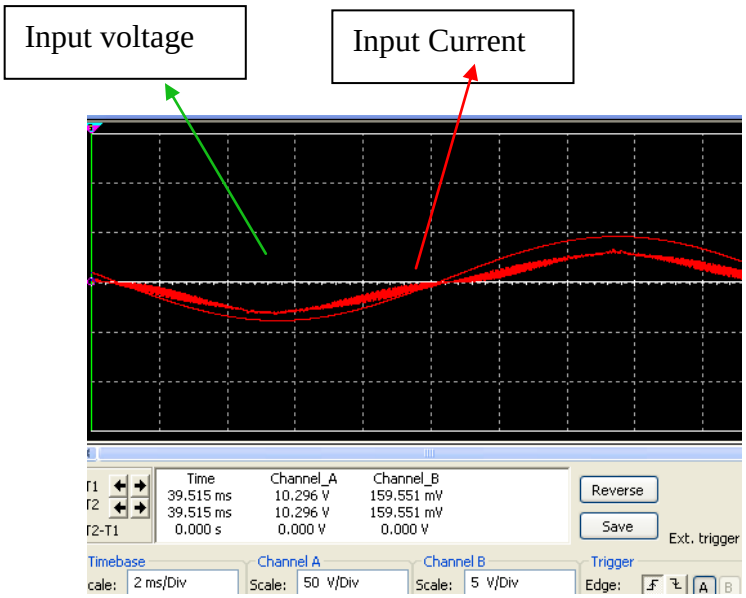

Fig. 12: Waveform showing input voltage and input current waveform showing power factor correction

Since the circuit is operated in boundary condition mode, the input current is forced to track the input voltage there by increasing the power factor (Tsorng-Juu Liang *et al*., 2012).

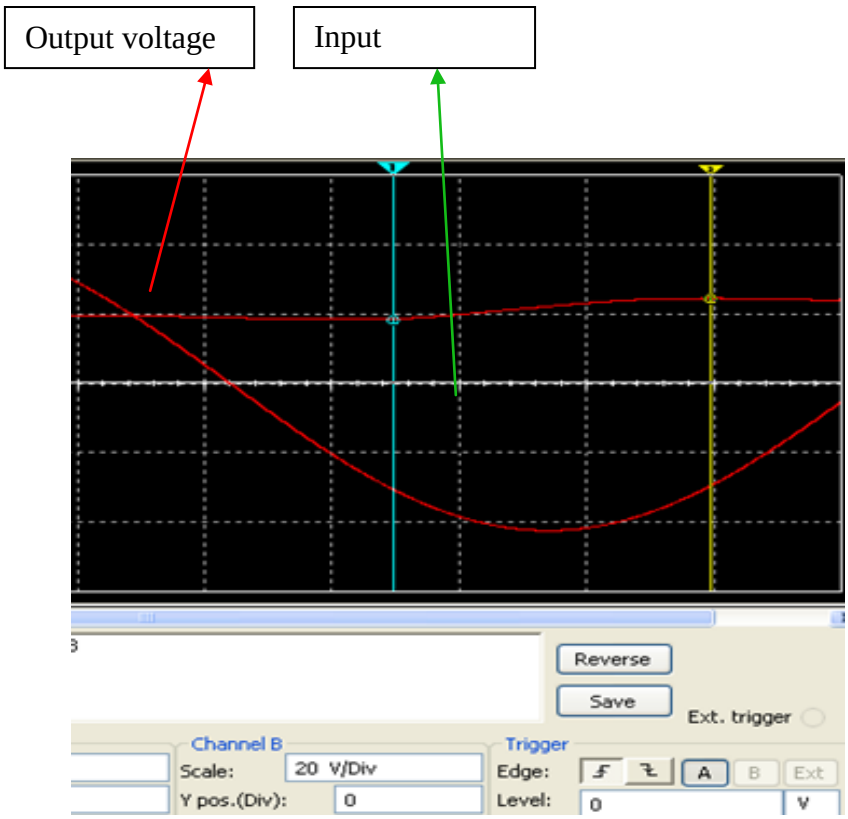

Fig. 13: Output and input voltage waveforms (input voltage =30v, output voltage=54v)

Conculsion:

Interleaved dual BCM PFC controllers operate two parallel-connected boost power trains 180° out of phase. Interleaving extends the maximum practical power level of the control technique from about 300W to greater than 800W. Unlike the continuous conduction mode (CCM) technique often used at higher power levels, BCM offers inherent zero current switching of the boost diodes, which permits the use of less expensive diodes without sacrificing efficiency In this paper power MOSFET can be triggered by simple astable multivibrator circuit using IC 555 timer,& it output is inverted using NOT gate so that it meet the major requirement of phase difference for MOSFET instead of imported IC like FAN9611/12,& also using low value coupled inductor leakage inductance can be reduced & PFC can be achieved &also cost will reduced. From the simulated result it can be concluded that we can maintain output constant by providing feedback circuit.

REFERENCES

Ahsanuzzaman, S.S., Timothy MCRae, Mor M. Peretz, Aleksandar Prodic, 2012. " Low volume Buck converter with Adaptive inductor core Biasing'', Applied Power Electronics Conference and Exposition (APEC), 2012, IEEE Trans. 978-1-4577-1216.

Doo-Yong Jung, Young-Hyok Ji, Jun-Ho Kim, Chung-Yuen Won and Yong-Chae Jung, 2010. "Ripple Analysis of Interleaved Soft Switching Boost Converter for Photovoltaic Applications'' International Power Electronics Conference (IPEC), IEEE Trans. 978-1-4244-5394.

Hanju Cha, Woojong Lee, Tae-pung An, 2011. "Design and Implementation of 50kW Multi-String Photovoltaic PCS Using three-phase interleaved DC-DC converters'', Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011), IEEE Trans. 978-90-75815-15-3.

Hiroyakikosai, Seana McNeal, Biswajit Ray, 2011. "Design &implementation of compact interleaved Boost converter'' , IEEE Trans.

Ho, C.N.M., H. Breuninger, S. Pettersson, G. Escobar, L. Serpa, and A. Cocci, 2011. "Practical Implementation of an Interleaved Boost Converter using SiC Diodes for PV Applications.'' 8th International Conference on Power Electronics and ECCE Asia (ICPE & ECCE), IEEE Trans, 978-1-61284-956.

II-Oun Lee and Gun-Woo Moon, 2013. "Soft-Switching DC/DC Converter with a Full ZVS Range and Reduced Output Filter for High-Voltage Applications'' IEEE Trans. on power electronics, 28: 1.

Jen-Ta Su, Chih-Wen Liu, Chuan-Sheng Cheng, and Chung-Wen Hung, 2012. "A Self-Calibration Scheme for Improved Current Share of Multiphase DC-DC Converter,'' Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE Trans. 978-1-4577-1216.

Jun-yin, G.U., W.U. Hong-Fei, Chen Guo-cheng, 2010."Research On Photovoltaic Grid-Connected Inverter Based On Soft-Switching Interleaved Fly back Converter'' 5th IEEE Conference on Industrial Electronics and Applications (ICIEA), 15-17 June 2010, IEEE Trans. 978-1-4244-5046.

Pyosoo Kim, Sanghyuk Lee, Junsung Park and Sewan Choi, 2011. "High Step-up Interleaved Boost Converters Using Voltage Multiplier Cells'', 8th International Conference on Power Electronics and ECCE Asia(ICPE & ECCE), IEEE Trans. 978-1-61284-957.

Tsorng-Juu Liang, Senior Member, IEEE, Shih-Ming Chen, Lung-Sheng Yang, Jiann-Fuh Chen, 2012. "Ultra-Large Gain Step-Up Switched-Capacitor DC-DC Converter With Coupled Inductor for Alternative Sources of Energy" IEEE Trans. 1549-8328, on Circuits and Systems I: Regular Papers, IEEE Transactions on 59: 4.