ISSN:1991-8178

Australian Journal of Basic and Applied Sciences

Journal home page: www.ajbasweb.com

Low Power High Performance (LPHP) SRAM Cell for Write Operation

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ARTICLE INFO

Article history:
Received 12 November 2014
Received in revised form 26 December 2014
Accepted 29 January 2015
Available online 10 February 2015

Keywords:
SRAM, write margin, power, delay, SNM and write ability

ABSTRACT

Background: Presently, living in a predominantly electronics world, the current technology requires lower system power consumption for many applications, due to dramatic growth in applications that consume less power and high performance. Power consumption plays vital role in mobile devices and battery powered portable electronic system. The conventional 6T SRAM cell is susceptible in power consumption. **Objective:** To propose new Low power High Performance SRAM architecture to reduce the power consumption during write 0 and write 1 operation because the cache write consumes considerable large power due to full voltage swing on the bit-line. **Results:** The simulated results shows the write power consumption reduced approximately 77.4% and faster response compared to the Conventional 6T SRAM cell due to single Bit Line (BL) technique during write operation. Both read delay and static noise margin are maintained same as the 6T cell after carefully sizing of all the transistors. **Conclusion:** In the proposed cell, the two extra transistors to connect or disconnect the feedback connection between the two back to back inverters during write operation and hence the write activity factor is reduced which makes the proposed cell consumes less power during write operations compared with the conventional cell.

To Cite This Article: C.M.R. Prabhu and K. Ramanathan, Low Power High Performance (LPHP) SRAM Cell for Write Operation. ***Aust. J. Basic & Appl. Sci.,*** *9(5): 176-180, 2015*

INTRODUCTION

Advances in chip design using CMOS technology have made possible the design of chips with high integration, fast performance, and low power consumption (Sheng Lin *et al*., 2008). Static Random Access Memory (SRAM) continues to be one of the most fundamental and vitally important memory technologies today. As process technology is scaled down, threshold voltage and leakage current variations are increased (Gupta,V *et al*., 2010). The increasing market of mobile devices and battery-powered portable electronic systems is creating demands for chips that consume the smallest possible amount of power. Static random access memories (SRAMs) consist of almost 90% of very large scale integrated (VLSI) circuits. The power consumption and speed of SRAMs are important issues that have led to multiple designs with the purpose of minimizing the power consumption during both read and write operations (Grossar,E *et al*., 2006). Due to this, design of power-efficient high-performance SRAM cell has gained importance (Prabhu, C.M.R *et al*., 2013) and acknowledging that write-power consumption is higher than read-power consumption. Many authors have introduced various techniques to overcome this major issue in a different manner. The proposed cell focuses on increasing the speed- of-write operation by reducing power consumption and access delay.

The main goal of this paper is to introduce the SRAM cell which can perform the write operation faster. It is similar to a Novel 7T SRAM Cell for low-power cache design (Ramy, E *et al*., 2005) except has one additional PMOS transistor. Both have feedback path transistors to cut off the cross-coupled inverter's path before any write operation. This way, the write operation can be done easily by transferring the value from bit-line to storage node. Therefore, the power consumption and access time can be reduced significantly. The results and simulations are compared with conventional 6T to show the high performance of this new cell. The rest of the paper is organized as follows: Section 2 presents the architecture of proposed SRAM cell followed by the simulation results, discussion and conclusions in section 3 & 4, respectively.

Proposed circuit description:

The architecture of the proposed cell is shown in figure 1. The proposed schematic contains eight transistors as a replacement for Conventional 6T.

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The proposed SRAM cell is different from the conventional 6T by having extra one PMOS and one NMOS transistor (P3 andN5) at the feedback path of the inverter, as given in the figure below. The extra transistor's hardware burden can be tolerated by providing low power consumption and reduced access delay. The switching operation for these two feedback path transistors is controlled by nW and W signals. These feedback path transistors are used to make immediate state change for storage nodes Q and nQ without discharging completely. The word line (WL) is here to enable the write '0' operation. R is to enable the write '1' and read operation. All the results were obtained in a 0.12µm CMOS technology at room temperature with 1.2V supply voltage using Microwind3 tool.

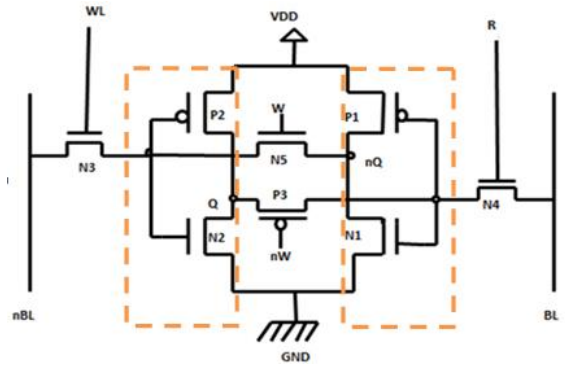
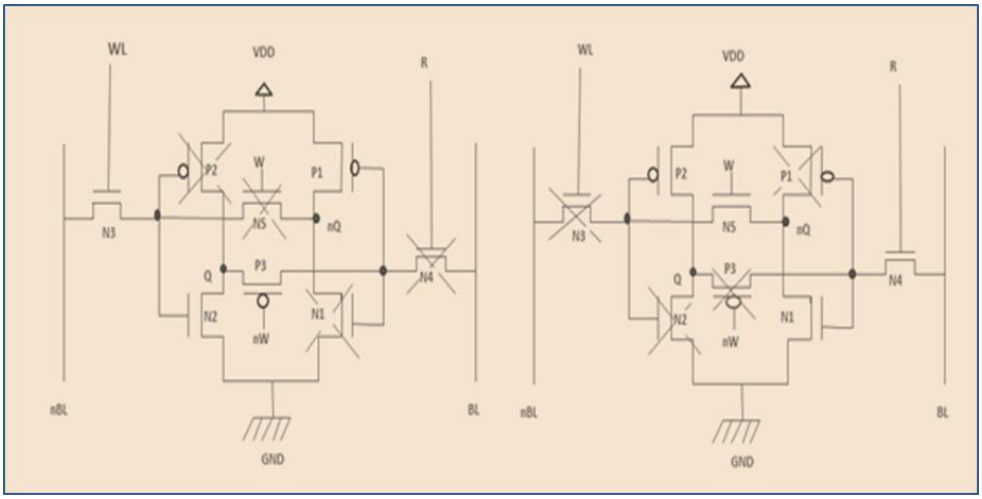
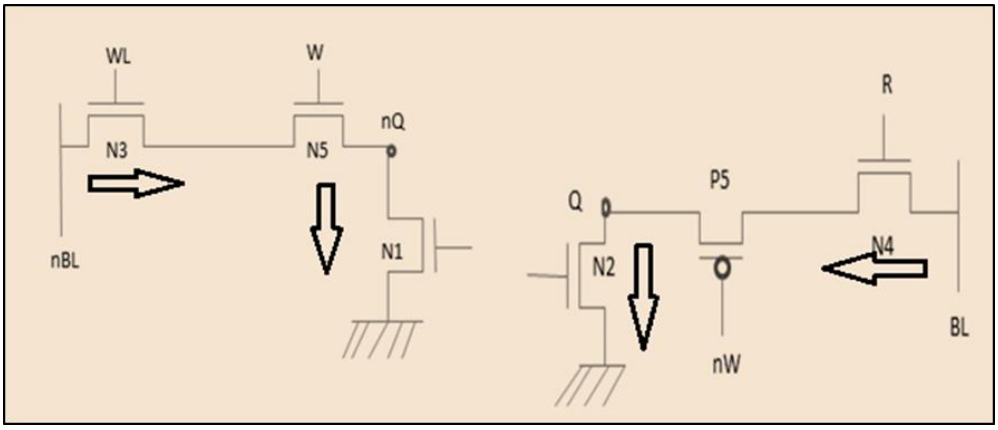


Fig. 1: LPHP SRAM cell.



(a) (b)

Fig. 2: Write circuit (a) cell state from "1"->"0" and (b) cell state from "0"->"1"



(a) (b)

Fig. 3: Critical read path when (a) nQ= "0" and (b) Q = "0"

Write'0' and write '1' operations are achieved by choosing appropriate values in bit lines (BL and nBL). Write operation starts by turning OFF or ON both of the feedback path transistors alternatively. In write'1' mode, the storage node Q should be written as High by setting BL='1'and WL kept Low. Both feedback path transistors P3 and N5 are ON mode and turning OFF N3 through the gate signal W to Low. R is then enabled to High. Since the feedback connection is disconnected it's easy to transfer the value from BL to Q. The charge at nQ will discharge through N1 and for this low value P2 will be ON and N2 will be OFF. So the charge will be stored at Q. To write'0' at storage node Q , transistors P3 and N5 will be OFF mode followed by turning OFF the transistor N4 through gate signal R to low. Bit lines (BL and nBL) are discharged and charged. Next, WL is asserted to high. Since N5 is turned OFF, the feedback loop is disconnected. The data going to be written is predicted by bit line voltage, since N1 is OFF and disconnects the pull-down path which pushes nQ to high and will not let Q to fully discharge.

In the read mode, normally bit lines (BL and nBL) are pre-charged in advance for any read operation. Throughout the read operation the cell acts as conventional 6T and N5 is kept ON by making W high followed by setting R to be High logic level. Read"0" occurs when Q is holding "0" by having N4, P3 and N2 (Figure 3b) in the read path which indicates that bit line voltage dropped. During read"1" operation nQ is holding"0" by connecting the transistors N3, N5 and N1 (Figure 3a) by maintaining the pre-charged value in the bit line.

Simulation results and discussions:

The proposed SRAM cell been analysed under various criteria such as write ability, speed, power consumption and access delay. The new proposed architecture is designed and implemented using Microwind3 in 0.12µm CMOS technology. Simulation for the analysis using BSIM4 model with VDD=1.2V. Considering an additional two feedback path transistors to connect or disconnect the coupled inverters, it's made easy to flip the storage node states. So the write operation can be done easily without discharging the bit line entirely. The simulated results for different inputs such as 0->1, 1->1, 1->0 and 0->0 are shown in Table1. The overall power consumption for the proposed cell is small compared to Conventional 6T, especially for 1->0 and 0->1 transition due to the minimal voltage drop at bit lines by cutting off the feedback loop. Huge power reduction of 77.4% and 77.7% can be observed. For a write operation, the write delay is defined as the time between the activation 50% of WL to when Q bar is 90% of its full swing. The write delay approximately equals the propagation delay of inv2 (P2 and N2) and inv1 (P1 and N1). Table 2 shows the comparison of write delay for transition 1->0 and 0->1. Since no transition occurred in 0->0, 1->1 can be ignored. The new proposed cell has lower delay while Conventional 6T is higher due to lower charging or discharging time in bit line. It happened due to the presence of one of the feedback path transistors, by disconnecting the loop to make immediate state change in storage nodes. Figure 5 signifies lower write power in proposed cell compared to conventional 6T for different supply voltages.

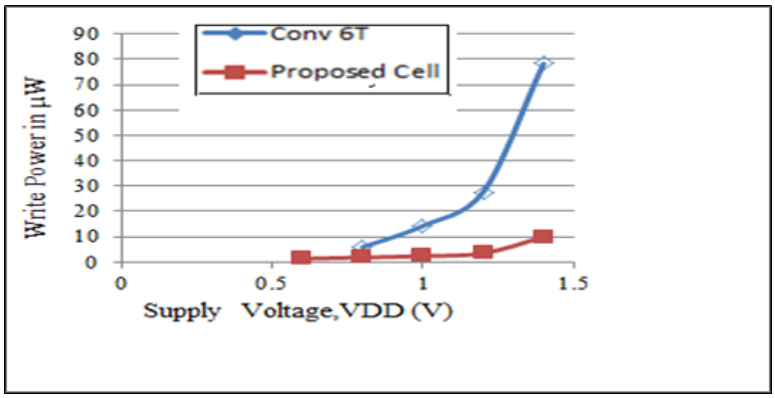


Fig. 5: Power dissipation.

Table 1: Summary of Write power for different input.

Power consumption (µw)			
Transitions	Conv.6T cell	7T SRAM cell	Proposed Cell
0—>1	30.699	31.672	6.940
1—>1	0.002	0.0026	0.0006
1—>0	30.695	6.839	6.847
0—>0	0.002	0.0015	0.0005

Table 2: Summary of Access Time.

Access Time(ps)			
Transitions	Conv.6T cell	7T SRAM cell	Proposed cell
0—>1	111	117	66
1—>0	111	62	64

Table 3: Temperature vs Hold Power.

Temperature °c	Hold Power(nW)	
	Conv.6T	Proposed Cell
27	15	6
50	33	10
75	52	21
100	93	41
125	154	73
137	197	96

Table 4: SNM for different VTH.

SNM(mv)		
VTH	Conv.6T	Proposed Cell
0.3	-	105
0.4	195	165
0.7	-	395

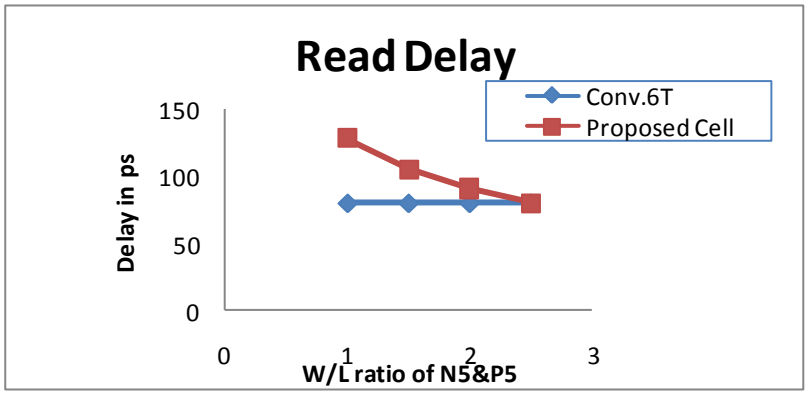


Fig. 6: Read delay varies with different W/L ratio.

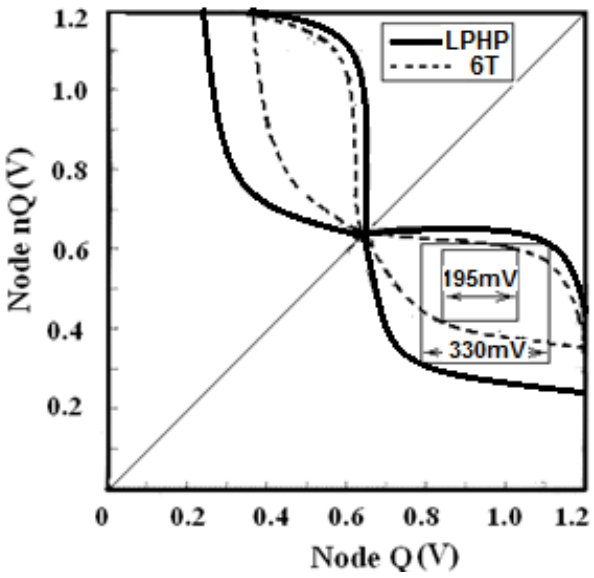


Fig. 7: Graphical representation of SNM.

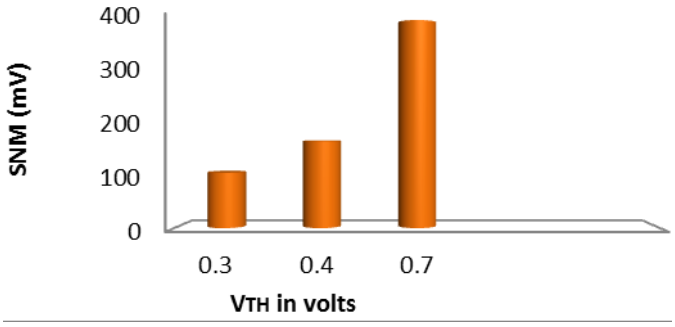


Fig. 8: SNM for different Vth.

The result of temperature on write operation for the conventional 6T and the proposed cell are shown in Table3. The results indicate that power consumption of proposed cells is lower compared to Conventional 6T, also that the proposed cell is capable of function up to T=137^{o}C .The disadvantage of this cell, read power consumption, is higher than the Conventional 6T of about 11% due to the additional transistors in the feedback loop. Read delay for both read '0' and read '1' is higher than the conventional 6T due to the read path consisting of three transistors which is in ON mode. So it takes a longer time to discharge through the bit lines. By increasing the W/L ratio of the feedback transistors read delay can be minimized. As seen from the Figure 6, Read delay is equal to the 6T cell at W/L ratio of 2.5 which shows enlarging the width of the feedback transistors can compensate the degradation in the read access delay.

The first consideration in the SRAM cell design is the stability to hold data (Chang, Y *et al*., 2004). The cell stability can be measured as read stability and static noise margin (SNM). The SNM is defined as the maximum DC noise voltage required to flip the cell- stored data (Prabhu, C.M.R *et al*., 2010 and Seevinck, E *et al*., 1987)to measure the SNM by plotting the curve for node Q and node nQ voltages. This technique is called butterfly (or VTC) curve measurement. Figure8 shows the butterfly curve of the proposed cell and Conventional 6T.The simulated results in table4 shows that the SNM of a proposed cell is 1.7 times higher than Conventional 6T. Figure7 highlights the improvement of the SNM for different threshold voltage varies from 0.3V to 0.7V. At VTH =0.44V, when enlarging the width of W/L to 2.5, the SNM of 330mV is attained while SNM of Conventional 6T is 195mV. The proposed cell has a short write pulse which is useful to avoid instability.

Conclusions:

In this proposed cell, the performance is improved in terms of power consumption and delay factors by introducing the two extra transistors to connect and disconnect the feedback path. The simulation result shows that the cell can be power-efficient and high-speed in write operation by reducing the write power up to 77.4% as well as the access delay reduced up to 42.3% .The improvement in SNM indicates the proper sizing adjustment for the extra transistors and better write ability compared to conventional 6T.

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