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A High Gain and Low Noise Figure for Dual Band LNA with Notch Filter

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ABSTRACT

This paper presents the design and analysis of a dual-band concurrent low noise amplifier (LNA) for 2.4 / 5.75 GHz wireless applications. This LNA combines a notch filter and T-matching network with inductive degenerated topology at the single stage common-source transistor. The LNA used two stage of GaAs HEMT by cascading the transistor to improve the gain and noise figure (NF). The LNA is matched concurrently at the two frequency bands by matching the input and output networks. The simulation results showed a high gain $|S_{21}|$ of 33 dB and 28.7 dB and low NF of 0.46 dB and 0.54 dB for center frequency of 2.4 GHz and 5.75 GHz. The supply voltage for LNA is 2V. Simulation of the design was performed with the Advanced Design System (ADS) software. The design is especially suitable for use in multi-standard wireless front end receiver.

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INTRODUCTION

Today, many telecommunication gadgets such as Wi-Fi, WiMAX, LTE and mobile phones offer multi band coverage with dual-band, tri-band even quad-band which required multiplication by the channel of the receiver. The advantage of using multi band compared with single band is to reduce drop calls and network busy interference. In addition, dual band phone has better sound quality than a single band phone. With dual band capability, the front end receiver was able to make a WiFi and WiMAX operate simultaneously. Therefore, it is of high demand to design for multi band in future.

The multi band frequency in single chip currently helps a lot in designing and improving the size of die and power consumption. In fact the multi band design also helps to minimize the packaging and testing costs (Spiridon, 2012). Many of the researchers choose to use complementary metal oxide semiconductor (CMOS) technology to design the LNA topology such as (Huang, 2013; Dehqan, 2011; Gupta, 2010; Si Xiong, 2010; Low Li Lian, 2011).

Since the technology of semiconductor device grows strongly, the bipolar junction transistor (BJT) and CMOS is no longer an option. There are additional high-frequency semiconductor substrates, including FET families such as metal oxide semiconductor FET (MOSFET), metal semiconductor FET (MESFET), high electron mobility transistor (HEMT) and pseudomorphic HEMT (PHEMT) as alternative selection.

The FET fabricated with these semiconductor materials offer a wide range of performance capabilities for example from low NFs to high output powers and from the high-frequency (HF) range through millimeter-wave frequencies. Table 1 shows the performance of the characteristics of a microwave transistor with several semiconductor devices (Pozar, 2012). With their excellent performances in high-power operations at microwave frequencies, HEMT family is the next-generation RF/microwave power amplifier (Jie Liu, 2007).

This paper introduces new combination techniques and topology to improve the dual band LNA concurrently for wireless telecommunications purposed.The LNA design uses GaAs HEMT as

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amplifier to obtain high gain, low NF conditions and consume low power.

This paper discussed new dual band concurrent LNA cascaded using T- matching network with notch filter and inductive degenerated topology design. Derivation of input and output matching network and analysis of notch filter is presented.

Table 1: Performance characteristics of microwave transistors (Pozar, 2012).

Device	BJT	HBT	CMOS	MESFET	HEMT	HEMT
Semiconductor	Si	SiGe	Si	GaAs	GaAs	GaN
Frequency range (GHz)	10	30	20	60	100	10
Typical gain (dB)	10–15	10–15	10–20	5–20	10–20	10–15
NF (dB)	2.0	0.6	1.0	1.0	0.5	1.6
Power capacity	High	Medium	Low	Medium	Medium	High
Single-polarity supply	Yes	Yes	Yes	No	No	No

Dual Band Lna Design And Matching Network:

Many methods and techniques have been implemented to obtain a receiver working simultaneously on different standards. In particular, several kinds of multi band LNAs have been designed such as switches LNA (Huang, 2013), parallel LNA (Ahsan, 2012), concurrent LNA (Dehqan, 2011) and wideband LNA (Liang, 2010). Each kind of design has to guarantee that the LNA parameters suitable with the wireless standard required by IEEE or 3rd Generation Partnership Project (3GPP). Therefore, this paper introduces a design and analysis of new techniques concurrent dual band LNA which improves the performance of previous works.

Fig.1 shows the proposed schematic of concurrent dual band LNA with two stage amplifier (M1 and M2). T-matching is used as input matching network and notch filter as an output matching network. The single stage amplifier for single LNA has been designed using T-matching for both input and output matching network. Then, the amplifier was cascaded to enhance the power gain. The output of the second stage amplifier which includes notch filter circuit will produce dual band frequencies.

The NF is a critical part of the system. To maintain at the minimize value which is near to NF min specification. Most of the researcher focus on those parts which can be acceptable by front-end communication standard, especially on the signal to noise ratio (SNR). One of the approach is by applying the inductor degenerated topology at transistor M1, a better NF reduction can be achieved (Andreani, 2001). If the initial value of NF is already high on the first stage, it is possible the noise would become higher in the system if cascade or cascode be implemented.

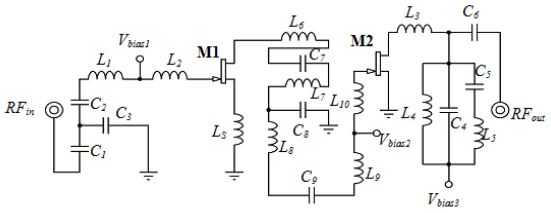

Fig. 1: Schematic of the proposed Dual Band LNA for wireless applications.

The function of the input and output decoupling capacitors $C_1$and $C_6$is toblock the direct current (DC) from the input and output lines while allowing passage of RF signals.

Meanwhile, the capacitors C_3 and C_8 are known as bypass capacitors. The capacitors bypass AC noise and allow pure DC signals to pass through the circuits. It also prevents the unwanted communication between devices sharing the same power source. The capacitors bypass the high frequency generated by the input signal. High quality type of capacitor ceramic chip with low series inductance must be chosen for C_3 and C_8 to bypass the noise of RF signal through the circuits.

The microwave transistor must be biased at an appropriate operating point to achieve a proper operation. The GaAs HEMT DC bias voltage must be applied to both gate and drain, without disturbing the RF signal paths; and it can be done with biasing and decoupling circuitry for a dual-polarity supply (Pozar, 2012). Fig.2 shows the schematics of the DC bias voltage to the transistor gate (M1 and M2) and transistor drain (M2). The schematic of Fig.2 is based on (Othman, 2013) designed.

The capacitors C_{A1}, C_{A2} and C_{A3} are bypass capacitors. This capacitor is typically polarized tantalum or electrolytic capacitor type because it is only for low frequency signals. Usually, these capacitors should be placed as close as possible to the power supply to obtain maximum effect.

The RF chokes, L_{A1},L_{A2} and L_{A3} are used in the DC bias voltage. The function of the RF chokes is to

provide a low DC resistance for biasing, and provides high impedance at RF frequencies which isolates the signal from the bias supply.

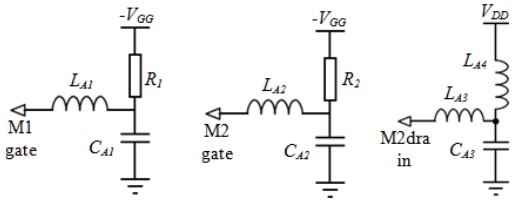

Fig. 2: Schematic of the DC bias voltage to transistor gate and drain.

Input Matching Design:

The maximum power transfer from the source and the load can be obtained by matching the optimum design of input and output network. This can be realized when choosing the best input matching network. Currently there are several types of matching network has been used by researchers to design the system such as Π matching network, L matching network and Ladder matching network. For this design we proposed T-matching network for input impedance. The T- matching network gives the best performance to optimize the gain and NF with minimum power consumption (Othman, 2012). In order to achieve better input matching for both bands, a T-match network with C_1, C_2 and C_3 are used at the input. At the same time, L_1 and L_2 are added to build the required output capacity in the design.

Additionally, the single stage of this LNA is constructed by using inductor degenerated topology. This topology reduces the interaction between output and input stage; and can be separately optimized to improve the reverse isolation (Low Li Lian, 2011). The equivalent circuit of the first stage of transistor M1 is shown in Fig.3. Assume that the simplified model of the transistor M1 is unilateral, and that internal component such as R_i,R_{ds}, C_{gd} and C_{ds}can be ignored.

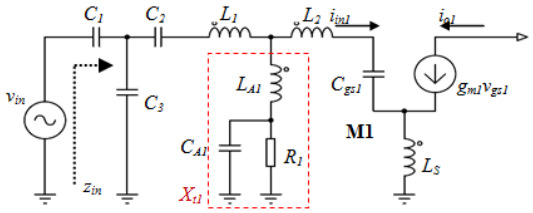

Fig. 3: The equivalent circuit of the transistor M1 in common-source stage.

The V_{bias1} of transistor gate M1 is essentially zero because of elements in the small signal AC model. Thus, let X_{t1} be the equivalent circuit of V_{bias1} and the equation can be derived as equation (1).

where

$$X_{t1} = \left(\frac{1}{j\omega C_{A1}} \| R_1\right) + j\omega L_{A1} \tag{1}$$

The output current, i_{o1} for the equivalent circuit can be derived as equation (2) and input voltage, v_{in} as equation (3):

where

$$i_{o1} = g_{m1} v_{gs1} = g_{m1} i_{in1} \left(\frac{1}{j\omega C_{gs1}}\right) \tag{2}$$

$$v_{in} = i_{in1}\left[\left(j\omega L_2 + j\omega L_s + \frac{1}{j\omega C_{gs1}}\right) + g_{m1}\left(\frac{1}{j\omega C_{gs1}}\right) j\omega L_s\right] \tag{3}$$

The input impedance,Z_{in} can be derived as equation (4) with the Im(Z_{in}) and Re(Z_{in}) at input impedance as below:

$$Z_{in} = \left(\left[\left[\left(j\omega L_2 + j\omega L_s + \frac{1}{j\omega C_{gs1}}\right) + g_{m1}\left(\frac{1}{j\omega C_{gs1}}\right) j\omega L_s\right] \| X_{t1}\right] + j\omega L_1 + \frac{1}{j\omega C_2}\right] \left\| \frac{1}{j\omega C_3}\right) + \frac{1}{j\omega C_1} \tag{4}$$

where

$$Im(Z_{in}) = \left(\left[\left[\left(j\omega L_2 + j\omega L_s + \frac{1}{j\omega\, C_{gs1}}\right) \| X_{t1}\right] + j\omega L1 + 1j\omega C21 j\omega C3 + 1j\omega C1 = 0\right.\right. \quad (5)$$

and

$$Re(Z_{in}) = \frac{g_{m1} L_S}{C_{gs1}} = 50\Omega \quad (6)$$

The real part of input impedance, Re(Z_{in}) must be equal to 50Ω in order to have impedance matching for maximum power transfer to transistor M1. The imaginary part of input impedance, Im(Z_{in}) gives the frequency of interest which can be set according to L_1, L_2, L_S, C_1, C_2, C_3 and C_{GS} parameters. The input of source impedance, Z_S for two frequency bands can be seen in the Smith Chart at Simulation Results.

Output Matching Design:

Fig.4 shows the equivalent circuit of the second stage transistor M2 and the combination of notch filter on the output matching network. Two notched frequency bands are obtained by embedding a series of LC branch in parallel with the parallel LC (LC tank). The filter used at the output matching network to suppress the interference frequency at 2.4 GHz and 5.75 GHz without affecting the NF of the LNA.

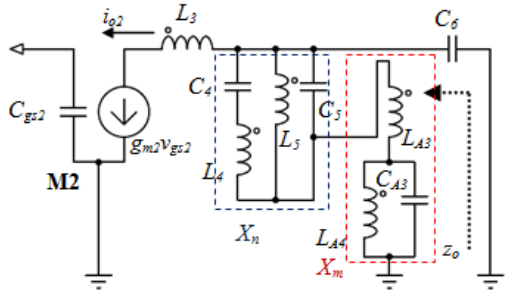

Fig. 4: Theequivalent circuit of the second stage of transistor M2 with notch filter.

The V_{bias3} of transistor M2 is essentially zero because of elements in the small signal AC model. Thus, let X_m be the equivalent circuit of V_{bias3} and can be derived as equation (7).

$$X_m = \left(j\omega L_{A4} \left\| \frac{1}{j\omega C_{A3}}\right.\right) + j\omega L_{A3} \quad (7)$$

The notch filter equation X_n for the equivalent circuit at the output matching network can be calculated as follows:

where

$$X_n = \left(j\omega L_4 + \frac{1}{j\omega C_4}\right) \left\| j\omega L_5 \right\| \frac{1}{j\omega C_5} \quad (8)$$

Both equations (7) and (8) are in a series circuit, thus we can add (7) and (8) and simplify the equation as X_{t2}.

$$X_{t2} = X_n + X_m \quad (9)$$

The output current, i_{o2} for the small signal model can be derived as equation (10) and the output voltage, v_o can be derived as equation (11):

where

$$i_{o2} = -g_{m2} v_{gs2} = -g_{m2} i_{in2} \left(\frac{1}{j\omega C_{gs2}}\right) \quad (10)$$

and

$$v_o = -g_{m2} i_{in2} \left(\frac{1}{j\omega C_{gs2}}\right)\left(j\omega L_3 + \left[X_{t2} \left\| \frac{1}{j\omega C_6}\right.\right]\right) \quad (11)$$

The output impedance,Z_o can be derived at output impedance as equation (12):

$$Z_o = \left(j\omega L_3 + \left[\left(\left(\left(j\omega L_{A4} \left\| \frac{1}{j\omega C_{A3}}\right.\right) + j\omega L_{A3}\right) + \left(\left(j\omega L_4 + \frac{1}{j\omega C_4}\right) \left\| j\omega L_5 \right\| \frac{1}{j\omega C_5}\right)\right) \| \frac{1}{j\omega C} \right. \right. \quad (12)$$

From imaginary part of output impedance Im(Z_o) gives matching frequency which is to be set as frequency of interest, according to L_3, L_4, L_5, L_6, C_4, C_5, and C_6 parameters. The output of load impedance, Z_L for two frequency bands can be seen in the Smith Chart at Simulation Results.

Notch Filter Analysis:

Fig.5 shows a notch filter structure to attenuate the interferences. The notch filter is placed after the gain stage to avoid the decline in NF due to the loss of this filter (Liang, 2010).

The power gain $|S_{21}|$ versus frequency with different values of L_4 are depicted in Fig.6. When the values of L_4 are changed, the $|S_{21}|$ at the frequency 1 GHz to 3.5 GHz also varies with different values as

shows in Fig.6. But at the same time, there is no change at the high frequency range from 4 GHz to 8 GHz. In LC tank (L_4 and C_4), if the value of L_4 is large and the value C_4 is low, the total reactance will be high and the amount of current circulating in the tank will be small. Thus the graph will shift in resonant frequency to the left. If the value of L_4 is low, the reactance becomes low and the amount of current circulating in the tank will be much greater and the graph will shift in resonant frequency to the right. Five different values L_4 with the interval of 0.1nH has been simulated. The simulation values of L_4 are 0.6909nH, 0.7909nH, 0.8909nH, 0.9909nH and 1.0909nH. The Fig.6 depicts that with the large L_4 value, the target frequency center, which is 2.4 GHz can be produced.

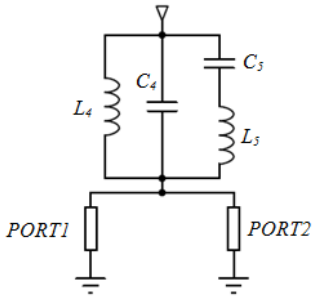

Fig. 5: Biasing circuit for notch filter.

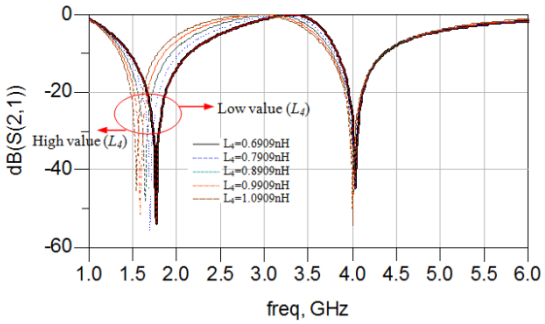

Fig. 6: Simulated power gain (S_{21}) for different value of L_4 at parallel LC circuit.

The output $|S_{21}|$ variation in the frequency range between 4 GHz to 8 GHz is depicted in Fig.7. The simulation shows that five different values of L_5has been simulated. The simulation values of L_5 are 1.3311nH, 1.4311nH, 1.5311nH, 1.6311nH and 1.7311nH. When the value L_5 is high, the output of $|S_{21}|$ shifts in resonant frequency to the left with the frequency notch at 3.5 GHz. But if the value L_5 is low, the output of $|S_{21}|$ shift in resonant frequency to the right at frequency notch 4 GHz.

The DC bias voltage, V_{bias3} is connected to the notch filter circuit at the output matching network as depicted in Fig.4. The graph can be tuned to the desired output by tuning both notches simultaneously by varying the L_{A3} values. Fig.8 shows the total output bandwidth when the L_{A3} has been tuned with eight different values. The output results show that the inductor, L_{A3} will lock the frequency bandwidth and the graph will shift in resonant frequency to the left when the L_{A3} values are high, while if the values of L_{A3} is low the graph shift in resonant frequency to the right.

Simulation Results:

The fully concurrent dual band LNA for 2.4 GHz and 5.75 GHz has been simulated by ADS 2008 software using GaAs HEMT transistors. The measurement of dual band LNA is carried out for NF and gain. From the simulation, the source impedance matching, Z_S is 33.59 + j21.00Ω at 2.4 GHz and 46.42 + j3.25Ω at 5.75 GHz. Meanwhile the output impedance matching Z_L is 76.15 + j14.81Ω at 2.4 GHz and 31.98 + j 16.84Ω at 5.75 GHz. The impedance matching simulation is depicted in Fig.9.

Fig.10 and Fig.11 shows NF at the different frequency bands. The NF is 0.46 dB at 2.4 GHz and 0.54 dB at 5.75 GHz. The LNA's noise performance has a lower value and it can be accepted.

Fig.12 and Fig. 13 shows the measured and simulated of power gain $|S_{21}|$ versus frequency. The simulation results show that the gain of LNA at 2.4 GHz and 5.75 GHz is 33 dB and 28.7 dB, respectively.

The following Table 2 summarizes the comparison and performance of previous work of dual band LNA with this present work. It proves that this work demonstrates and achieved the highest gain

with lowest NF reduction compared with the previously published dual band LNA.

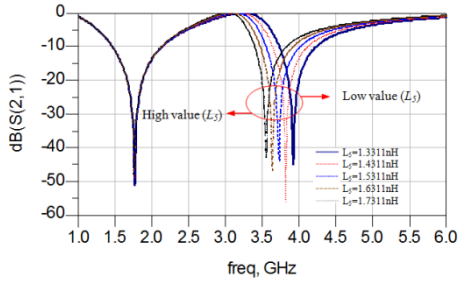

Fig. 7: Simulated power gain (S_{21}) for different value of L_5 at series LC circuit.

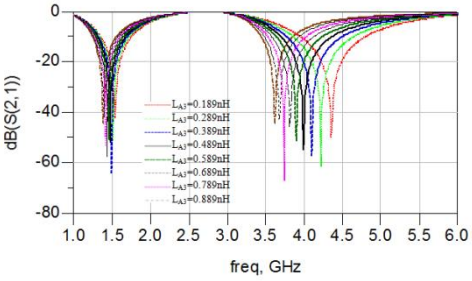

Fig. 8: Simulated power gain (S_{21}) for different value of L_{A3} at V_{bias3} circuit.

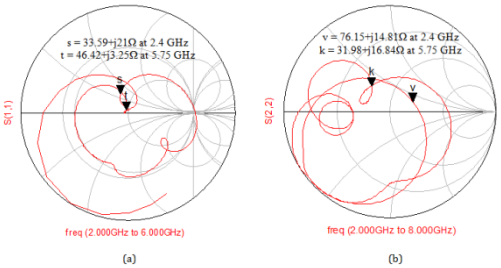

Fig. 9: Simulated a) source impedance matching, Z_S 2.4 GHz and 5.75GHz and b) load impedance matching, Z_L 2.4 GHz and 5.75GHz.

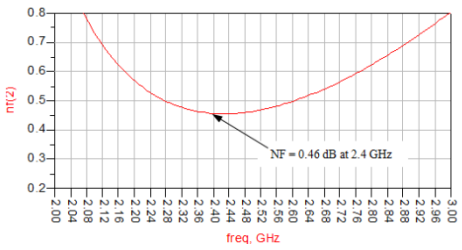

Fig. 10: Simulated NF at 2.4 GHz.

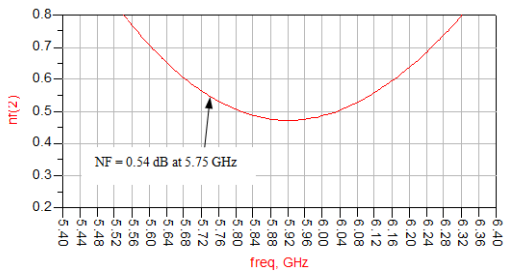

Fig. 11: Simulated NF at 5.75 GHz.

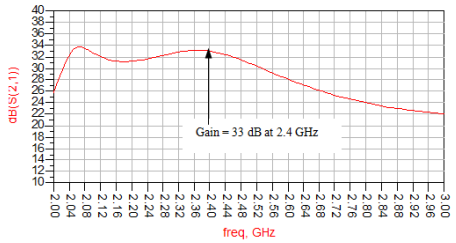

Fig. 12: Simulated $|S_{21}|$ at 2.4 GHz.

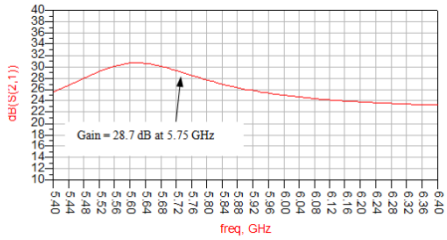

Fig. 13: Simulated $|S_{21}|$ at 5.75 GHz.

Table 2: Performance NF and $|S_{21}|$ and comparison of previously reported dual band LNA.

Specification	[3]		[4]		[7]		This work	
Freq. (GHz)	2.4	5.2	2.4	5.2	2.4	5.2	2.4	5.75
S_{21} (dB)	14.2	13.1	23.76	21.41	26.2	21.8	33.0	28.7
NF (dB)	2.9	2.6	1.9	1	2.07	1.84	0.46	0.54
Voltage (V)	0.7		3.3		NA		2	

Conclusion:

A new concurrent dual band LNA capable of simultaneous operation at two different frequency bands is introduced. It uses cascading technique and inductive generated topology to develop the architecture of the LNA. This design also includes a T-matching of the input matching network and notch filter for the output matching network which has two band frequencies. The effectiveness of the proposed design achieved a superior NF and $|S_{21}|$ over previously published concurrent LNA. The LNA has two pass bands and can be used for Wi-Fi and a WiMAX/LTE application. It also can be used for larger office areas, indoor and outdoor, or full sized house that suited for areas that require more accessibility.

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REFERENCES

Ahsan, N., A. Ouacha, J. Dabrowski, C. Samuelsson, 2007. Dual Band Tunable LNA for Flexible RF Front End. Applied Sciences & Technology, IBCAST, 19-22.

Andreani, P., H. Sjoland, 2001. Noise optimization of an inductively degenerated CMOS low noise amplifier. Circuits and Systems II: Analog and Digital Signal Processing, 48: 835-841.

Othman, A.R., A.B. Ibrahim, M.N. Husain, A.H. Hamidon and J. Hamidon, 2012. Low Noise Figure of Cascaded LNA at 5.8 GHz Using T-Matching Network for WiMAX Applications. 2012 International Journal of Innovation, Management and Technology (IJMIT), 3: 688-691.

Othman, A.R., K. Pongot, Z. Zakaria, M.K. Suaidi, A.H. Hamidon, 2013. Low Noise Figure and High Gain Single Stage Cascoded LNA Amplifier With Optimized Inductive Drain Feedback for WiMAX Application. International Journal of Engineering and Technology (IJET), 5: 3.

Ch.Liang, P., Rao, T. Huang and Sh.Chung, 2010. Analysis and Design of Two Low-Power Ultra-Wideband CMOS Low-Noise Amplifiers With Out-Band Rejection. IEEE Trans. Micro Wave Theory and Tech, 58: 277-286.

Dehqan, A.R., Mafinezhad, Khalil, E. Kargaran, H. Nabovati, 2011.Design of low voltage low power dual-band LNA with forward body biasing technique.Electronics, Circuits and Systems (ICECS), 591-594.

Gupta, S.K., A. Garg, N.P. Singh, 2010. Design and simulation of an improved dual band LNA for

WLAN applications.Computer and Communication Technology (ICCCT), 678-682.

Huang, C..W.P., J. Soricelli, Lui Lam, M. Doherty, P. Antognetti, W. Vaillancourt, 2013. Novel silicon-on-insulator SP5T switch-LNA front-end IC enabling concurrent dual-band 256-QAM 802.11ac WLAN radio operations.Radio Frequency Integrated Circuits Symposium (RFIC), 133-136.

Jie Liu, Yugang Zhou, Jia Zhu, Yong Cai, Kei May Lau, K.J. Chen, 2007. DC and RF Characteristics of AlGaN/GaN/InGaN/GaN Double-Heterojunction HEMTs. Electron Devices, 54: 1-2.

Low Li Lian, N.M. Noh, M.T. Mustaffa, A.B.A. Manaf, O.B. Sidek, 2011. A dual-band LNA with 0.18-µm CMOS switches. Micro and Nanoelectronics (RSM), 172-176.

Pozar, M., David, 2012. Microwave Engineering, 4th ed., John Wiley & Sons.

Spiridon, S., C. Dan and M. Bodea, 2012. Overcoming the Challenges of Designing CMOS Software Defined Radio Receivers Front-Ends Embedding Analog Signal Conditioning. 2012 13th Int. Conf. Optim.Electr.Electron. Equip, 1: 1207-1210.

Si Xiong, Yumei Huang, Zhiliang Hong, 2010. A dual-band 2.1GHz/5.2GHz LNA for reconfigurable radio," Solid-State and Integrated Circuit Technology (ICSICT), 710-712.