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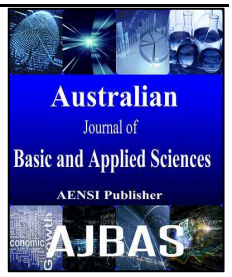

Assessment of Fixed and Variable Amplitude Bipolar Carriers for a 1Φ Ternary Multilevel Inverter

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ABSTRACT

Inverters are used to convert DC input voltage to AC output voltage of desired magnitude and frequency. This project presents a new group of ternary DC source 9-level inverter. The proposes a ternary multilevel inverter to comparison of bipolar multicarrier pulse width modulation (PWM) techniques. Nowadays multilevel inverters have become more popular over the years in high electric applications due to reduced switching losses, low costs, low harmonics distortion and high voltage capability when compared to traditional PWM inverters. Various bipolar PWM strategies like phase disposition (PD) strategy, phase opposition and disposition (POD), alternate phase opposition disposition (APOD) strategy and Variable Frequency(VF) strategy with equal amplitude carriers and unequal amplitude carriers have been developed using MATLAB-SIMULINK and tested for different modulation indices ranging from 0.8-1 for equal amplitude carriers and 0.6-1 for unequal amplitude carriers for the chosen single phase cascaded ternary multilevel inverter.

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INTRODUCTION

The main function of a multilevel inverter is to produce a desired AC voltage waveform from several levels of DC voltages. These DC voltages may or may not be equal to one another. The features of multilevel inverter are they can generate output voltages with extremely low distortion, they draw input current with very low distortion and it can operate at both fundamental switching frequency and high switching frequency PWM. Nabae *et al* (1980) proposes a new neutral-point-clamped Pulse Width Modulation (PWM) inverter composed of main switching devices which operate as switches for PWM and auxiliary switching devices to clamp the output terminal potential to the neutral point potential has been developed. This inverter output contains less harmonic content as compared with that of a conventional type. Two inverters are compared analytically and experimentally. In addition, a new PWM technique suitable for an ac drive system is applied to this inverter. The neutral-point-clamped PWM inverter adopting the new PWM technique shows an excellent drive system efficiency, including motor efficiency, and is appropriate for a wide-range variable-speed drive system. Carrara *et al* (1992) developed a pulse width modulation (PWM) subharmonic method to control single-phase or three-phase multilevel voltage source inverters (VSI) is considered. An analytical expression of the spectral components of the output waveforms covering all the operating conditions is derived. The analysis is based on an extension of Bennet's method. The improvements in harmonic spectrum are pointed out, and several examples are presented, which prove the validity of the multilevel modulation. Jose Rodriguez *et al* (2002) presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, and space-vector modulation. Keith *et al* (2004) introduced a new type of multilevel inverter is introduced which is created by cascading two three-phase three-level inverters using the load connection, but requires only one dc voltage source. This new inverter can operate as a seven-level inverter and naturally splits the power conversion into a higher-voltage lower-frequency inverter and a lower-voltage higher-frequency inverter. This type of system presents particular advantages to Naval ship propulsion systems which rely on high power quality, survivable drives. New control methods are

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described involving both joint and separate control of the individual three-level inverters. Azli and Choong (2006) developed a new type of multilevel inverter is introduced which is created by cascading two three-phase three-level inverters using the load connection, but requires only one dc voltage source. This new inverter can operate as a seven-level inverter and naturally splits the power conversion into a higher-voltage lower-frequency inverter and a lower-voltage higher-frequency inverter. This type of system presents particular advantages to Naval ship propulsion systems which rely on high power quality, survivable drives. New control methods are described involving both joint and separate control of the individual three-level inverters. Roozbeh Naderi and Abdolreza Rahmati (2008) discussed about phase-shifted carrier (PSC) pulsewidth modulation (PWM) in its conventional form is a good solution for single-phase Cascaded inverters as alternative phase opposition disposition (APOD) PWM for single-phase diode clamped inverters. PSC distributes the switching angles of APOD PWM waveform among the legs uniformly and reduces the switching frequency of each leg. This paper proposes a modified PSC technique based on partly shifted carriers for all disposition types including phase disposition (PD) which is suitable for three-phase cascaded inverters. Simulation results are also included for using carrier-based space-vector PWM (SVPWM). Mariuz Malinowski *et al* (2010) present a survey of different topologies, control strategies and modulation techniques used by these inverters. Regenerative and advanced topologies are also discussed. Khoucha *et al* (2011) discusses a comparison study for a cascaded H-bridge multilevel direct torque control (DTC) induction motor drive. Cougo *et al* (2011) paper is to show that they may be applied to parallel converters using interleaving techniques, given that these converters also have multilevel characteristics. PWM methods based on carriers' disposition and on zero sequence injection are studied for parallel multilevel inverters. Gupta and Jain (2012) introduced a new topology for multilevel DC-AC conversion is presented in this study. It consists of isolated symmetric input DC sources alternately connected in opposite polarities through power switches. The structure allows synthesis of multilevel waveform using reduced number of power switches as compared to the classical topologies. Masaoud *et al* (2013) developed a new configuration of a three-phase five-level multilevel voltage-source inverter is introduced. The proposed topology constitutes the conventional three-phase two-level bridge with three bidirectional switches. A multilevel dc link using fixed dc voltage supply and cascaded half-bridge is connected in such a way that the proposed inverter outputs the required output voltage levels. The fundamental frequency staircase modulation technique is easily used to generate the appropriate switching gate signals. Palanivel and Dass (2014) various carrier pulse width modulation techniques are proposed, which can minimise the total harmonic distortion and enhances the output voltages from five level inverter. Three methodologies adopting the constant switching frequency (CSF), variable switching frequency (VSF), and phase shifted pulse width modulation (PSPWM) concepts are proposed in this paper. The above methodologies divided into two techniques like subharmonic pulse width modulation which minimises total harmonic distortion and switching frequency optimal pulse width modulation which enhances the output voltages. Gabriel *et al* (2014) This paper proposes novel multilevel ac/dc/ac converters with reduced number of semiconductor devices to achieve light weight, efficiency, and better input current quality. Lim *et al* (2015) proposes a new approach of modular-cell inverter with a reduced number of flying capacitors (RFCI) using hybrid carrier-based pulsewidth modulation (PWM) named as phase-shifted carrier phase-disposition PWM (PSC-PD-PWM). The novel multilevel inverter topology is designed by clamping a series of modular cell onto a low-operational-frequency cell. Rasilo *et al* (2015) The effect of multilevel inverter supply on power losses in magnetic cores and electrical machines is studied. A dynamic numerical model for the hysteresis, eddy current, and excess losses in a core lamination is first developed. By both measurements and simulations for a ring-core inductor, we demonstrate how increasing the number of inverter voltage levels decreases the iron losses when compared with traditional two-level supply. Rathore and Edpuganti (2015) deals with synchronous optimal pulse width modulation (SOP) permits low switching frequency modulation of multilevel inverter for medium-voltage high-power industrial ac drives without compromising on total harmonic distortion (THD). An aim of our experiment was to operate a nine-level cascade inverter of an induction motor drive at an average device switching frequency limited to rated fundamental frequency by using SOP technique. To reduce the number of separate dc sources, a three-level diode clamped converter was used as a cell in the nine-level cascade inverter. Reddy *et al* (2014) discussed a generalized multilevel inverter (MLI) with frontend dc-dc conversion stage followed by a synchronized H-bridge is presented. By using this configuration along with the proposed embedded control, any desired number of levels (n) in the output voltage can be produced. The dc-dc conversion stage employs an asynchronous buck converter. The duty cycle of dc-dc converter is varied in the form of m-level piecewise constant (PWC) unidirectional sine wave to produce a similar output voltage across the dc-link capacitor. Roberge *et al* (2015) suggested a parallel algorithm on graphics processing unit for harmonic minimization in multilevel inverters.

Selvamuthukumaran *et al* (2015) discussed a hybrid multicarrier modulation to reduce leakage current in a transformerless cascaded multilevel inverter for photovoltaic systems. Vekhande *et al* (2015) proposed a switching state vector selection strategies for paralleled multilevel current-fed inverter under unequal dc-link currents condition. Xiao *et al* (2015) introduced a modular cascaded h-bridge multilevel pv inverter with distributed mppt for grid-connected applications.

Multi Level Inverter:

The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are 2*n*+1, where *n* is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. One of the advantages of this type of multilevel inverter is that it needs less number of components comparative to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two former types. Figure. 1 shows the power circuit for ternary DC source multi level inverter. It looks like a traditional cascaded H-bridge multilevel inverter except input dc sources using Vdc and 3Vdc. It can synthesize nine output levels; -4Vdc, -3Vdc, -2Vdc, -Vdc, 0, Vdc, 2Vdc, 3Vdc, 4Vdc. Expected output voltage level is n and number of H bridge $V_n = 3^n$, Where n = 1,2,3,…. n. The lower inverter generates a fundamental output voltage with three levels and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves, here the final output voltage levels becomes the sum of each terminal voltage of H-bridge. The advantages of ternary inverter is reduced number of dc source, Low switching losses, Flexibility of enhance the output voltage and Reduction in cost.

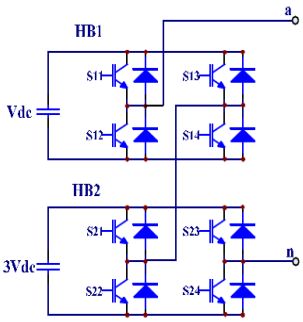

Fig. 1: Power circuit for single phase nine level cascaded multilevel inverter.

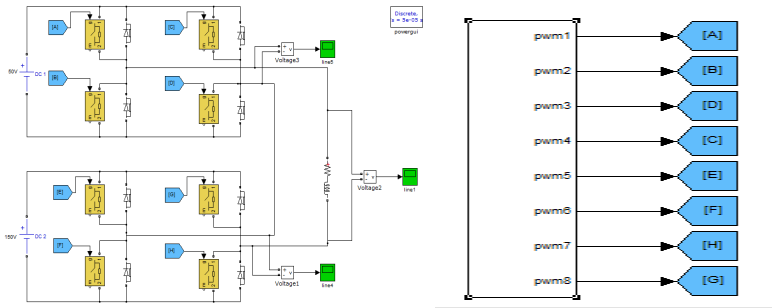

Fig. 2: Sample PWM generation logic model developed using SIMULINK for VFPWM technique.

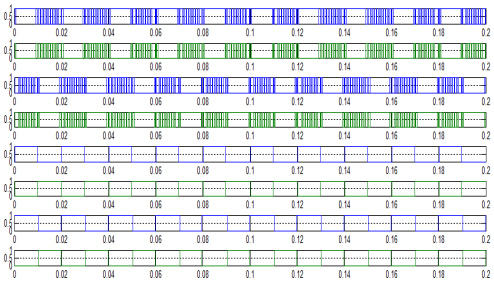

Fig. 3: PWM signal pattern for various switches.

Table 1: Comparison between symmetrical and asymmetrical inverters.

Comparison	Symmetrical inverter	Asymmetrical inverter	
		Binary	Ternary
Levels	2N+1	2^{N+1}-1	3^N
DC sources	N	N	N
Switches	4N	4N	4N

Table 2: Switching table for nine level output.

V_{out}	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}
$4V_{dc}$	1	0	0	1	1	0	0	1
$3V_{dc}$	0	1	0	1	1	0	0	1
$2V_{dc}$	0	1	1	0	1	0	0	1
V_{dc}	1	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
$-V_{dc}$	0	1	1	0	0	1	0	1
$-2V_{dc}$	1	0	0	1	0	1	1	0
$-3V_{dc}$	0	1	0	1	0	1	1	0
$-4V_{dc}$	0	1	1	0	0	1	1	0

Modulation Strategies:

Several CFDs exist in multi-carrier PWM strategies for MLIs. These strategies have more than one carrier option that can be triangular, saw tooth, a new function etc. As far as the particular carrier signals are concerned, there are multiple CFDs including function, frequency, amplitude, phase of each carrier and offset between carriers. Although multilevel inverter offers several advantages, the control strategies of MLI are quite challenging due to the complexity to cater the transitions between the voltage levels (or steps). A number of modulation strategies are used in multilevel power conversion applications. In this proposed topology two methods are used.

1. Equal Amplitude Carriers
2. Un Equal Amplitude Carriers (or) Variable Amplitude Carriers (VAC)

3.1. Equal Amplitude Carriers:

In this method, all the triangular carriers used will have the same amplitude. The PWM methods used are PDPWM, PODPWM, APODPWM and COPWM with sine, THI, trapezoidal, TAR and stepped wave references. Fig. 2 to 4 shows the sample carrier arrangement, output voltage and FFT plot for VFPWM strategy with THI reference (m_a = 0.8 and m_f=20). Where m_a and m_f are the amplitude and frequency modulation index.

3.2. Un Equal Amplitude Carriers (or) Variable Amplitude Carriers (VAC):

In this method, all the triangular carriers used will not have the same amplitude. The PWM methods used are UEAPD (Un Equal Amplitude Phase Disposition) PWM, UEAPODPWM, UEAAPODPWM and UEACOPWM with sine, THI, trapezoidal and TAR references. Fig. 5 to 7 shows the sample carrier arrangement, output voltage and FFT plot for PDPWM strategy with sine reference (m_a = 0.8 and m_f=20). Figs. 8 to 10 show the sample reference waveforms. m_a is varied from 1 to 0.6 for equal amplitude carrier methods. In EAC method if m_a is varied from 1 to 0.51 then the inverter will work as a five level inverter and if the m_a is varied from 0.5 to zero then the inverter will work as a three level inverter. But in case of UEAC method if m_a is varied from 1 to 0.26 then the inverter will work as a five level inverter and if the m_a is varied from 0.25 to zero then the inverter will work as a three level inverter.

Where

$$m_a = \frac{A_m}{A_c} \quad (1)$$

$$m_f = \frac{f_c}{f_m} \quad (2)$$

m_{f1} - Frequency modulation index for upper and lower carriers.

m_{f2} - Frequency modulation index for intermediate carriers.

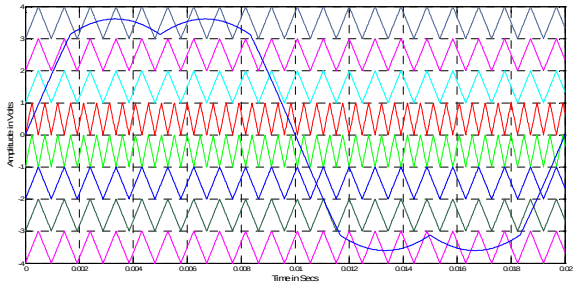

Fig. 4: Multicarrier arrangement for VFPWM technique.

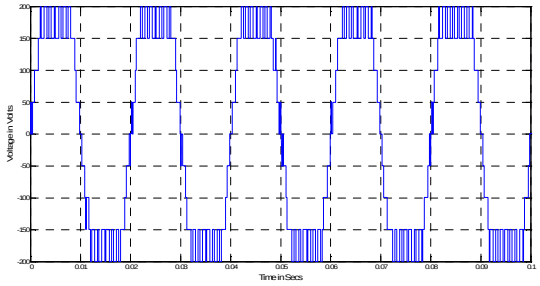

Fig. 5: Output voltage generated by VFPWM technique (THI ref.).

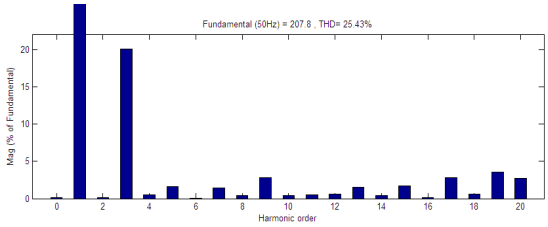

Fig. 6: FFT plot for output voltage of VFPWM technique (THI ref.).

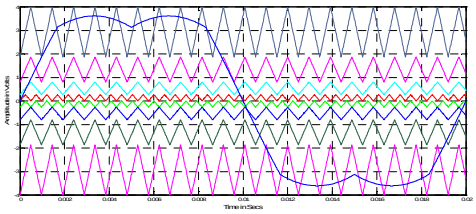

Fig. 7: Multicarrier arrangement for VAVFPWM technique.

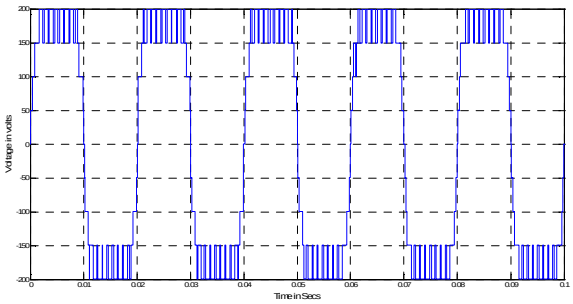

Fig. 8: Output voltage generated by VAVFPWM technique (THI ref.).

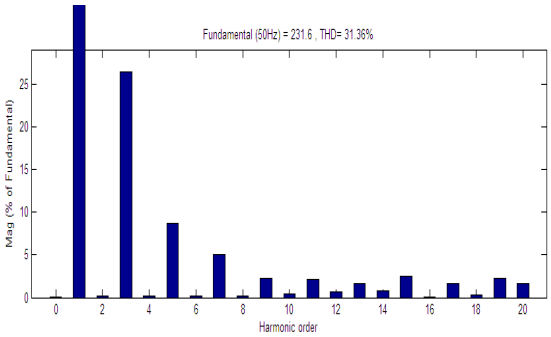

Fig. 9: FFT plot for output voltage of VAVFPWM technique (THI ref.).

Table 3: Comparison of various levels between EA carriers and UEA carriers.

Ref.	m_a	PWM techniques	
		PD	UEAPD
Sine, THI, 60 degree and Stepped wave reference	1	9-level	9-level
	0.9		
	0.8		
	0.7	7-level	
	0.6		
	0.5	5-level	7-level
	0.4		
	0.3		
	0.2	3-level	5-level
	0.1		
	>0 to < 0.09		3-level

Table 4: %THD for nine level output voltage based on equal amplitude and unequal amplitude carriers with various modulation indices.

Ref.	m_a	% THD for 9-level inverter							
		PDPWM		PODPWM		APODPWM		VFPWM	
		PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	VF	UEAVF
Sine reference	1	14.65	23.20	13.42	22.45	13.97	22.87	14.43	23.06
	0.9	17.38	24.73	16.03	23.50	16.64	23.98	17.39	24.60
	0.8	17.94	25.23	16.66	24.33	17.09	24.81	17.47	24.84
	0.7	7-level	23.41	7-level	24.07	7-level	24.09	7-level	23.07
	0.6		21.94		22.78		22.52		21.48
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								
THI reference	1	23.61	31.46	24.32	31.40	24.28	30.38	23.43	31.40
	0.9	25.58	31.44	25.65	32.03	25.83	32.05	25.43	31.36
	0.8	24.71	32.53	24.99	33.01	24.70	32.39	24.43	32.44
	0.7	7-level	32.47	7-level	33.09	7-level	32.73	7-level	32.38
	0.6		32.24		31.53		31.90		32.13
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								
Trapezoidal reference	1	17.75	26.33	17.50	27.51	17.71	26.96	17.52	26.55
	0.9	22.41	28.53	21.82	29.19	21.90	28.52	22.14	28.42
	0.8	20.97	29.69	21.80	30.29	21.78	29.97	20.48	29.60
	0.7	7-level	30.77	7-level	30.20	7-level	30.36	7-level	30.67
	0.6		30.33		28.95		29.47		30.20
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								
Stepped wave reference	1	13.42	23.82	12.27	22.37	12.65	22.56	13.19	23.82
	0.9	18.48	24.69	16.91	23.21	17.53	23.83	18.15	24.69
	0.8	19.82	24.04	18.09	23.56	18.45	23.86	19.15	24.04
	0.7	7-level	23.66	7-level	23.61	7-level	23.62	7-level	23.66
	0.6		21.90		22.47		22.54		21.90
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								

Table 5: V_{rms} for nine level output voltage based on equal amplitude and unequal amplitude carriers with various modulation indices.

Ref.	m_a	% THD for 9-level inverter							
		PDPWM		PODPWM		APODPWM		VFPWM	
		PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	VF	UEAVF
Sine reference	1	142.3	160.3	140.8	159.7	141.3	160.1	142.3	160.2
	0.9	127.1	153.5	127.8	153.2	127.6	153.4	127.1	153.5
	0.8	112.2	145.5	113.6	145.6	112.8	145.5	112.4	145.4
	0.7	7-level	138.3	7-level	138.5	7-level	138.5	7-level	138.3
	0.6		129.9		130.4		130.6		129.8
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								
THI reference	1	164	171.7	160.4	171.9	160.5	171.6	163.8	171.7
	0.9	146.9	163.8	147.3	164.3	147.4	164.2	146.9	163.8
	0.8	131.4	155.8	131	156.2	131.2	156	131.4	155.8
	0.7	7-level	148	7-level	148.1	7-level	148.1	7-level	148
	0.6		140.3		139.7		140		140.2
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								
Trapezoidal reference	1	165.8	171.9	165.4	172.7	165.5	172.4	165.8	171.9
	0.9	148.9	164.1	149	164.3	148.6	164.2	148.9	164
	0.8	131.9	156.1	132.3	156.2	132.1	156.2	132.1	156.1
	0.7	7-level	148.6	7-level	148.2	7-level	148.3	7-level	148.6
	0.6		140.2		139.6		139.8		140.2
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								
Stepped wave reference	1	142.6	159.9	141.7	160.1	142.2	160.4	142.6	159.9
	0.9	128.2	153.2	127.6	153.2	127.3	153.5	128.2	153.2
	0.8	112.1	145.5	113.4	145.3	112.3	145.1	112.3	145.5
	0.7	7-level	138	7-level	138.1	7-level	138.3	7-level	138
	0.6		130.2		130.2		130.2		130.2
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								

Table 6: V_{peak} for nine level output voltage based on equal amplitude and unequal amplitude carriers with various modulation indices.

Ref.	m_a	% THD for 9-level inverter							
		PDPWM		PODPWM		APODPWM		VFPWM	
		PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	VF	UEAVF
Sine reference	1	201.3	226.6	199.1	225.9	199.8	226.4	201.3	226.6
	0.9	179.7	217.1	180.8	216.6	180.5	216.9	179.7	217
	0.8	158.7	205.8	160.6	205.9	159.5	205.8	158.9	205.7
	0.7	7-level	195.6	7-level	195.9	7-level	195.8	7-level	195.5
	0.6		183.8		184.4		184.8		183.6
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								
THI reference	1	231.7	242.9	226.9	243.1	226.9	242.6	231.9	242.9
	0.9	207.8	231.6	208.5	232.3	208.3	232.3	207.8	231.6
	0.8	185.8	220.3	185.5	220.9	185.8	220.6	185.8	220.3
	0.7	7-level	209.4	7-level	209.4	7-level	209.4	7-level	209.3
	0.6		198.4		197.6		198		198.3
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								
Trapezoidal reference	1	234.5	243.1	233.8	244.2	234.1	243.8	234.5	243
	0.9	210.6	232	210.7	232.4	210.2	232.2	210.6	232
	0.8	186.6	220.8	187.1	220.9	186.8	220.9	186.8	220.8
	0.7	7-level	210.2	7-level	209.6	7-level	209.8	7-level	210.2
	0.6		198.2		197.4		197.8		198.2
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								
Stepped wave reference	1	201.7	226.1	200.4	226.4	201.1	226.8	201.6	226.1
	0.9	181.3	216.7	180.4	216.7	180	217.1	181.4	216.7
	0.8	158.6	205.7	160.4	205.4	158.8	205.3	158.8	205.7
	0.7	7-level	195.2	7-level	195.3	7-level	195.6	7-level	195.2
	0.6		184.2		184.1		184.1		184.2
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								

Table 7: DC component for nine level output voltage based on equal amplitude and unequal amplitude carriers with various modulation indices.

Ref.	m_a	% THD for 9-level inverter							
		PDPWM		PODPWM		APODPWM		VFPWM	
		PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	VF	UEAVF
Sine reference	1	0.56	0.06	0.69	0.55	0.0	0.28	0.43	0.06
	0.9	0.21	0.12	0.07	0.75	0.21	0.23	0.07	0.17
	0.8	0.39	0.06	0.62	0.36	0.16	0.24	0.24	0.24
	0.7	7-level	0.38	7-level	0.19	7-level	0.38	7-level	0.13
	0.6		0.14		0.07		1.08		0.00
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								
THI reference	1	0.22	0.31	0.28	0.36	1.76	0.72	0.32	0.41
	0.9	0.66	0.05	0.66	0.32	1.32	0.54	0.18	0.00
	0.8	0.61	0.00	0.00	0.11	0.74	0.06	0.00	0.06
	0.7	7-level	0.06	7-level	0.06	7-level	0.12	7-level	0.00
	0.6		0.06		0.63		0.25		0.00
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								
Trapezoidal reference	1	0.48	0.00	0.05	0.46	0.59	0.15	0.05	0.05
	0.9	0.30	0.11	0.06	0.22	0.06	0.16	0.18	0.11
	0.8	0.20	0.06	0.13	0.06	0.07	0.17	0.13	0.00
	0.7	7-level	0.00	7-level	0.60	7-level	0.24	7-level	0.06
	0.6		0.06		0.76		0.32		0.00
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								
Stepped wave reference	1	0.00	0.17	1.12	0.50	0.06	0.11	0.19	0.17
	0.9	0.07	0.29	0.55	0.69	0.21	0.12	0.00	0.29
	0.8	0.08	0.12	0.55	0.00	0.39	0.06	0.16	0.12
	0.7	7-level	0.00	7-level	0.06	7-level	0.26	7-level	0.00
	0.6		0.27		0.00		0.20		0.27
	0.5	5-level	7-level	5-level	7-level	5-level	7-level	5-level	7-level
	0.4								
	0.3								

Conclusions:

Various bipolar PWM strategies with equal amplitude carriers and unequal amplitude carriers have been developed using MATLAB-SIMULINK and tested for different modulation indices ranging from 0.8-1 for equal amplitude carriers and 0.6-1 for unequal amplitude carriers for the chosen single phase cascaded ternary multilevel inverter.

- It is observed from Table 4 that all PWM method provide output with relative low distortion for equal amplitude carriers. If equal voltage sources are chosen then the THD will be less in the case of unequal amplitude carriers. But for the unequal voltage sources the THD is more in the case of unequal amplitude carriers.
- It is observed from simulation results that (Table-5) almost in all the strategies unequal amplitude carriers gives more fundamental RMS values compared to equal amplitude carriers.
- It is seen from table 6 that peak voltage is more in the case of unequal amplitude carriers compared to equal amplitude carriers.

- It is observed from the table 7 that dc components are less in both equal and unequal amplitude carriers.
- The proposed PWM methods with less THD and higher RMS voltage can be implemented in industrial applications such as AC Power conditioners, static VAR compensators, drive systems, etc and in power generation industries.
- Various applications of ternary inverters are Induction heating, Aircraft power supply, HVDC, Motor drives, Electric utility application.

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