**Australian Journal of Basic and Applied Sciences**, 9(33) October 2015, Pages: 78-83

ISSN:1991-8178

**Australian Journal of Basic and Applied Sciences**

Journal home page: www.ajbasweb.com

# A New Multilevel Inverter Topology with Reduced Number of Switches for Photovoltaic Systems

S. Malathy and R. Ramaprabha

*Department of Electrical and Electronics Engineering, SSN College of Engineering, India.*

**ARTICLE INFO**

***Article history:***
*Received 3 October 2015*
*Accepted 31 October 2015*

***Keywords:***
*Basic unit, H-bridge, half height method, level generator, Multilevel inverter.*

**ABSTRACT**

Multilevel inverters are preferred over the conventional inverters for renewable energy interfaces. The stepped waveform and the increased number of levels at the output not only improve the harmonic spectrum but also reduce the stress on the semiconductor devices and filtering requirements. In this paper, a new topology for multilevel inverter that utilizes lesser number of switches is proposed. The working of the proposed topology along with the algorithm to determine the magnitudes of the dc sources are presented in detail. The proposed topology is compared with the conventional and few other existing topologies in terms of the number of switches and sources required to generate the specified number of steps at the output. The simulated and experimental results of the developed nine level inverter confirms the effectiveness of the proposed topology. The switching angles are determined by a fundamental frequency switching method called half height method.



**To Cite This Article:** S. Malathy and R. Ramaprabha., A New Multilevel Inverter Topology with Reduced Number of Switches for Photovoltaic Systems. ***Aust. J. Basic & Appl. Sci.,*** *9(33): 78-83, 2015*

## INTRODUCTION

Multilevel inverters (MLI) are well suited for applications requiring high power and medium voltages. The multilevel inverter uses a series of power semiconductor switches with one or more lower voltage dc sources to perform the power conversion. Capacitors, batteries, and renewable energy voltage sources like photovoltaic modules and fuel cells can be used as the multiple dc voltage sources. The concept of utilizing multiple small dc voltage sources to perform power conversion was patented by MIT researcher over twenty years ago (Fuller, J.F., 1988; Baker, R.H., 1975). The significant advantage of using several voltage levels is that it will lead to a better and more sinusoidal like output voltage waveform that results in lower harmonic distortion, reduced voltage stress across the switches and filtering requirements (Baker, R.H., 1980). Despite these advantages, the major disadvantage is that a multilevel inverter employs more number of semiconductor switches.

The conventional multilevel inverter topologies use either a single common source (neutral point clamped and flying capacitor topology) or multiple isolated dc sources (cascaded multilevel inverter topology) (Rodriguez, J.S., 2002). Though the diode clamped topology requires a single dc source, the number of clamping diodes required increases quadratically with the number of levels if the rating of the diode is chosen to be equal to that of the active switch. The clamping diodes are replaced by capacitors in flying capacitor topology leaving the control complicated besides increasing the overall size of the inverter (Lai, J.S. and F.Z. Peng, 1996; Escalante, M.F., 2002). The cascaded multilevel inverter topology (CMLI) is preferred over the others due to its modular nature, the flexibility and ease to extend. Cascaded multilevel inverters utilize H-bridge (full bridge circuit) and few such H bridges are cascaded to generate output with preferred levels. However, it results in the increase in number of switches, dc sources and other circuit components that in turn increases the overall size and cost of the system along with increased losses.

Many new topologies (Babaei, E., 2007; India IEEE International Conferenceon Power Electronics, 2012), with an aim to reduce the number of switches required have been reported in literature. This paper proposes a new topology that utilizes lesser switches and dc sources. The metrics are compared with that of the conventional and few optimized topologies in terms of number of switches, diodes, sources and voltage levels. The allied equations and the procedure to determine the voltage levels are also derived.

**Corresponding Author:** S. Malathy, Department of Electrical and Electronics Engineering, SSN College of Engineering, India
Tel: 9144- 27456700; E-mail: malathys@ssn.edu.in,

Australian Journal of Basic and Applied Sciences, 9(33) October 2015, Pages: 78-83

### *II. Conventional Topologies:*

The conventional form of CMLI consists of H-bridges and the number of levels required at the output determines the number of bridge units to be cascaded. Each bridge unit constitutes four unidirectional switches along with a dc source to generate two distinct voltage levels (+Vdc and -Vdc) besides a zero level. The CMLI is further classified either into symmetric or asymmetric depending on whether all the dc sources incorporated in the topology are of same value or not. In symmetric topology, the voltage levels of all the dc sources are identical whereas, in asymmetric topology the magnitudes of the dc sources are in a geometric progression of two (binary) or three (trinary). The number of switches, voltage levels and the maximum voltage of the inverter with k stages (H-bridge) are given by

$N_{switch} = 4k$ (1)

$N_{level} = 2k+1$, for symmetric CMLI (2)

$N_{level} = 2^{k+1}-1$, for asymmetric and binary progression (3)

$N_{level} = 3^{k}$, for asymmetric and trinary progression (4)

The maximum output voltage of the inverter with k stages is given by

$V_{o\,max} = \Sigma_i V_i$ , i=1,2,...,k (5)

This section substantiates the fact that more levels can be generated at the output without increasing the circuit components by suitably selecting the magnitude of the input dc sources. However, the major downside of CMLI is that it utilizes more number of switches and dc sources. Several new topologies have been proposed in literature which intend to generate more levels with reduced number of switches and sources. This paper proposes one such new topology, the working, and the algorithm to determine the magnitude of dc source voltage are presented in the next section.

### *III. The Proposed Topology:*

The basic unit and the sub module developed based on the basic unit are presented in Fig.1. The basic unit has a dc source and two unidirectional switches. One of the switches (S1) is connected in series with the source while the other (S2) is connected across the source-switch assembly. When the series switch is turned on, the output of the basic unit is +Vdc and the output is '0' when the parallel switch is turned on. Care must be taken that both the series and the parallel switches are not turned on simultaneously to avoid short circuiting the dc source.

Two such basic units are cascaded to form a sub_module. Besides, a third voltage source is added in the sub module. The structure of the sub module is shown if Fig.1.a. A sub module has three voltage sources and four uni directional switches. The switching status and the voltage levels that can be generated by the sub module are presented in Table I. The status of the switch is indicated by 0 and 1.

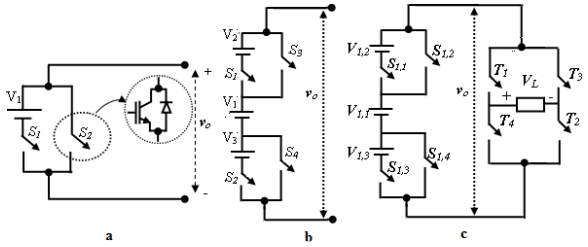


**Fig. 1:** a. Basic unit of proposed circuit b. sub module c. sub module with polarity generator.

**Table I:** Status Of Switches And Output Voltage Of Sub Module.

| State | Status of switch | | | | Output Voltage |
|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | |
| 1 | 0 | 0 | 1 | 1 | $V_1$ |
| 2 | 1 | 0 | 0 | 1 | $V_1+V_2$ |
| 3 | 0 | 1 | 1 | 0 | $V_1+V_3$ |
| 4 | 1 | 1 | 0 | 0 | $V_1+V_2+V_3$ |

The sub module can generate four positive voltage levels as shown in table I. To generate negative levels, a full bridge inverter (H-Bridge) is to be connected to the sub module as given in Fig.1.c and this set up can generate up to nine voltage levels as 0, $\pm V_{dc}$, $\pm V_1+V_2$, $\pm V_2+V_3$ and $\pm V_1+V_2+V_3$. The sub module determines the output voltage level while the H bridge determines the polarity. These sub modules can be cascaded further to generate more levels at the output. As mentioned earlier, these sub modules are capable of generating only positive levels and the series assembly of sub modules is called level generator and the H- bridge which decides the polarity is called the polarity generator. Turning on the switches $T_1$ and $T_2$ makes the voltage polarity positive and turning switches $T_3$ and T4 on makes the voltage polarity negative. Switches in the same leg of the H-bridge should not be turned on simultaneously. The extended structure of the proposed inverter with 'n' sub modules is shown in Fig.2. If the output voltage of the stages are $v_{01}$, $v_{02}$, ...,$v_{0n}$, the output voltage of the extended topology is

given by

$v_0(t) = vo_1(t) + v_{02}(t) +...+ v_{0n}(t)$ (6)

The required number of voltage sources, switches and the generated voltage levels at the output for the proposed extended topology with 'n' stages (sub modules) are given by

$N_{sources} = 3n$ (7)

$N_{switches} = 4n + 4$ (8)

$N_{levels} = 2^{2n+1} + 1$ (9)

The magnitudes of the dc voltage sources are to be chosen in such a way that maximum number of voltage levels is generated at the output. The generalized algorithm to determine the magnitudes of the dc voltage sources for a general structure with ' n' sub modules are given by

$V_{n,1} = V_{dc}/ n$ (10)

$V_{n,j} = 4^{i-1} (2^{j-2})V_{dc}$ ; i= 1,2,..n; j= 2 and 3 (11)

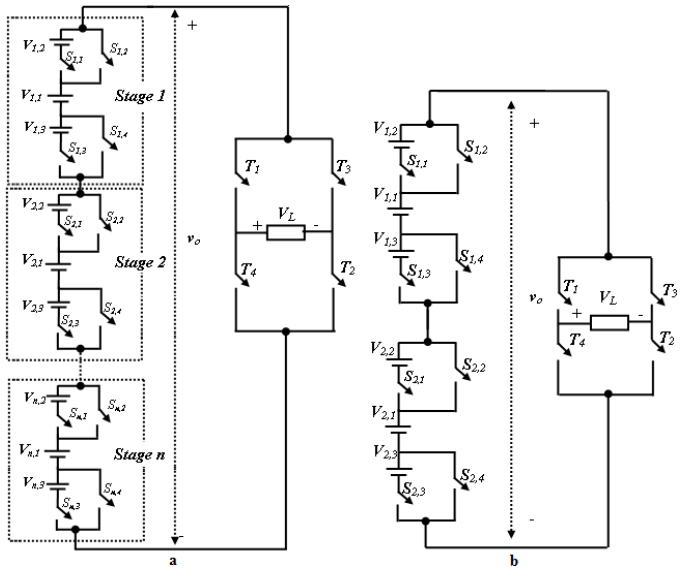


**Fig. 2:** a. Extended structure of proposed topology b. 33 level inverter.

A nine level inverter developed based on this topology is presented in Fig. 3. It has a single stage or sub module (n=1) and the magnitude of the three dc voltage sources are calculated as

$V_{1,1} = V_{dc}$ (11)

$V_{1,2} = V_{dc}$ (12)

$V_{1,3} = 2V_{dc}$ (13)

The voltage levels that can be generated are 0, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$ and $\pm 4V_{dc}$. The 33 level inverter developed based on the proposed topology is shown in Fig. 4. It has two cascaded stages or sub modules (n=2). The magnitudes of the voltages of the dc sources in the two stages are calculated as

***Stage 1:***

$V_{1,1} = V_{dc}/2$ (14)

$V_{1,2} = V_{dc}$ (15)

$V_{1,3} = 2V_{dc}$ (16)

***Stage 2:***

$V_{2,1} = V_{dc}/2$ (17)

$V_{2,2} = 4V_{dc}$ (18)

$V_{2,3} = 8V_{dc}$ (19)

The variety of dc sources required by this proposed topology can be calculated as

$N_{variety} = 2n+1$ (20)

The efficiency of the proposed algorithm is confirmed by testing a 9 level inverter developed based on this topology. The structure has 1 sub module and the magnitudes of the voltages are determined by the algorithm presented in section 3. Stage 1 voltages are chosen to be 10V, 10V and 20 V. The inverter has 4 unidirectional switches in the level generator part and four more unidirectional switches in the polarity generator part. The gating pulses to control the eight switches are generated at fundamental frequency by half height method.

This method calculates the main switching angles in such a way that the generated output approximates the sine wave. The switching angle is set when the function reaches the half- height of the level. The angles are determined by

$\alpha_i = \sin^{-1}((2i-1)/(m-1))$ (21)

where , i=1,2,...m-1/2 and m is the number of levels at the output.

Since the sine wave is both centrally symmetric and mirror symmetric, the switching angles for the first quadrant period ($0^0$ - $90^0$) are calculated. For an inverter output with m levels, there are (m-1)/2 main switching angles. Let $\alpha_i$ be the main switching angle, the angle in the second quadrant is $\pi-\alpha_i$, the angle in third quadrant is $\pi+\alpha$ and in the fourth quadrant it is $2\pi-\alpha_i$. The simulated output voltage waveform along with the spectral analysis is presented in Fig.3.

The output has nine distinct levels and the total harmonic distortion is 9.47%. The spectral quality can be improved further by cascading few sub modules and generating more levels at the output. As

the inverter is operated at fundamental frequency, the switching losses are less and as the spectral quality improves with levels, the burden on the filtering requirements is also reduced. The voltage across the basic units and the level generator unit are presented in Fig.4.

The experimnetal setup with the power circuit and the driver circuit along with the output voltage waveforms are shown in Fig.10. The magnitude of the three dc sources are calculated according to the algorithm presented in section 3. The pulses are generated by the microcontroller chipkit μC32 board and they are fed to the gates of the 8 IGBTs through the driver circuit with opto coupler isolation. The driver circuit is powered by the power supply circuit built with W10E rectifier IC, IC 7812 voltage regulator and filter capacitors. The load connected to the inverter is R load (50 Ω). The output voltage wavform presented in Fg.10.b is found to have 9 levels. The experimental results of the proposed topology complies with that of the simulation results.

The proposed topology is compared with the conventional topology and few other hybrid topologies reported in recent literature topologies in terms of the number of switches. The comparison results of the proposed inverter with the aforementioned inverters are presented in Fig.6. The number of switches required to generate the specific voltage levels are compared.

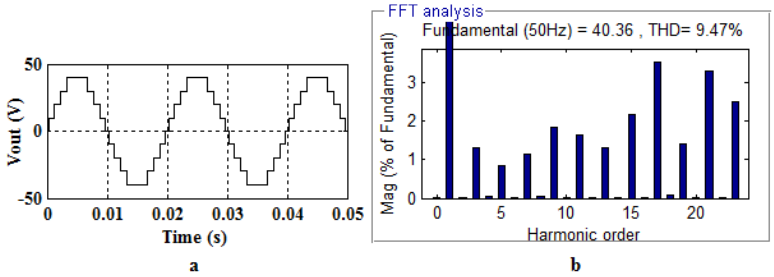


**Fig. 3:** a. Simulated results of 9 level inverter b. FFT analysis.

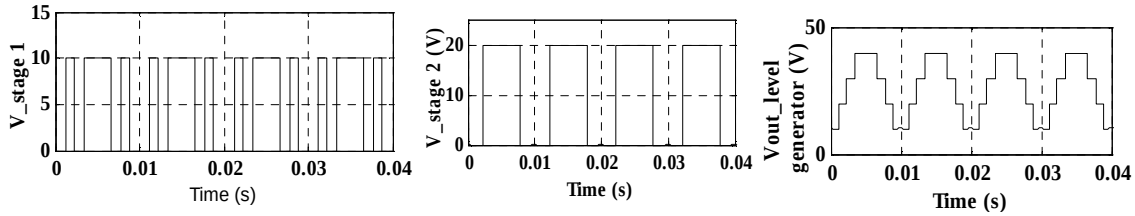


**Fig. 4:** a. Voltage at the individual stages.

**Fig. 5:** a. Experimental setup b. output voltage.

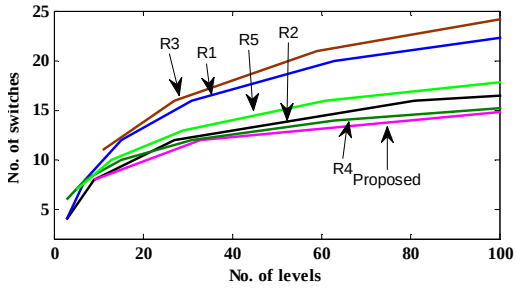


**Fig. 6:** Comparison results with other topologies.

The two asymmetric algorithms of the conventional MLI are represented as 'R1' and 'R2' in the Fig.5. They generate 2n+1-1 and 3n levels respectively with 4n switches. Topology reported in utilizes 5n+6 unidirectional switches and three asymmetric algorithms to generate different voltage levels. The third algorithm yields better results and is indicated by 'R3' in the comparison figure. Topology given in (Ebrahim Babaei, 2012) utilizes cascaded basic unit with unidirectional switches and a H-bridge to generate 2n+1-1 levels with 2n+4 switches and it is represented by 'R4'. The topology presented in [18] requires 3n+4 switches to generate 2n+2-3 levels and it is indicated by 'R5'. Topologies in makes use of a basic unit similar to that in (Ebrahim Babaei, 2012). However, in this topology each basic unit has a H-bridge circuit and several such sub modules are cascaded according to the requirement and it is indicated by 'R6'. The proposed topology can generate 22n+1+1 levels with 3n sources and 4n+4 unidirectional switches and it is represented by 'P' in Fig.6.

The Fig.6. clearly indicate that the conventional MLI topology requires more number of switches. The algorithm based on trinary progression results in the generation of more levels with less switches. A closer look on the figure however indicates that the proposed topology requires lesser number of switches than the conventional topology and other recently proposed topologies. But, the proposed topology requires additional sources. The availability of sources is however not an issue as renewable sources like fuel cells or solar cells can be easily interfaced with the proposed converter. Thus, it is evident that the proposed topology is superior to many existing topologies in terms of the voltage levels that can be generates and comparable with conventional topologies in terms of the source requirement.

### *IV. Conclusion:*

The paper has proposed a new multilevel topology with reduced number of IGBTs and dc sources. The working of the basic unit , sub module of proposed topology and the equations to calculate the input voltages are presented. Further, a 9 level inverter based on the proposed topology was developed and experimented. The simulation and the experimental results are in good agreement. The modular nature of the topology gives design flexibility and easy expandability and the number of voltage levels at the output can be increased without losing any levels by cascading more sub modules. The half-height PWM employed results in near sinusoidal like output and hence the harmonic distortion is less. This topology is suitable for PV interfaces as it requires multiple dc sources.

## ACKNOWLEDGMENT

The authors wish to thank the management of SSN College of Engineering, Chennai for providing all the computational and experiment facilities to carry out this work.

## REFERENCES

Fuller, J.F., E.F. Fuchs and K.J. Roesler, 1988. "Influence of harmonics on power distribution system protection." IEEE Trans. Power Delivery, 3: 549-557.

Baker, R.H., 1975. Electric Power Converter, U.S. Patent Number, 3: 867-643.

Baker, R.H., 1980. High-Voltage Converter Circuit, U.S. Patent No, 4: 203-151.

Rodriguez, J.S., Lai and F.Z. Peng, 2002. “Multilevel Inverters: Survey of Topologies, Controls, and Applications.” IEEE Transactions on Industry Applications, 49.4: 724-738.

Lai, J.S. and F.Z. Peng, 1996. “Multilevel Converters-A new Breed of Power Converters.” IEEE Trans. Ind. Applications, 32: 509-517.

Tolbert, L.M., F.Z. Peng and T. Habetler, 1999. “Multilevel Converters for Large Electric drives.” IEEE Trans. Ind. Applications, 35: 36-44.

Nabae, A., I. Takahashi and H. Akagi, 1981.“A New Neutral-point Clamped PWM inverter.” IEEE Trans. Ind. Applications IA., 17: 518-523.

Escalante, M.F., J.C. Vannier and A. Arzande, 2002. “Flying Capacitor Multilevel Inverters and DTC Motor Drive Applications.” IEEE Transactions on Industry Electronics, 49.4: 809-815.

IEEE Power Engineering Society Summer Meeting: Multilevel Converters as a Utility Interface for Renewable Energy Systems: [Proceedings of 2000 IEEE Power Engineering Society Summer Meeting] Tolbert, L. M. F. Z. Peng, 2000.

International Conference on Industrial Electronics, Control and Instrumentation. Cascade Multilevel Inverters for Utility Applications.[ Proceedings of 23rd International Conference on Industrial Electronics, Control, and Instrumentation]: Peng, F. Z. , J. W. McKeever, D. J. Adams, 1997.

Babaei, E., S.H. Hosseini, G.B. Gharehpetian, M. Tarafdar Haque and M. Sabahi, 2007.“Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology.” Electric Power Systems Research, 77: 1073–1087.

Babaei, E., 2010. " Optimal Topologies for Cascaded Sub-MultilevelConverters" Journal of Power Electronics, 10.3: 251-261.

Babaei, E., 2008. “A cascade multilevel converter topology with reduced number of switches.” IEEE Trans. Power Electronic, 23.6: 2657-2664.

Ebrahimi, J., E. Babaei, G.B. Gharehpetian, 2012. "A new multilevel converter topology with

reduced number of power electronic components." IEEE Trans. Ind. Electronics, 59.2: 655–667.

Luo, F.L. and H. Ye, 2010." Power Electronics: Advanced Conversion Technologies." Taylor & Francis group LLC.

Ebrahim Babaei, Sara Laali and Zahra Bayat, 2015. "A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches."IEEE Transactions on Industrial Electronics, 62.2.

Ebrahim Babaei, Mohammad Farhadi Kangarlu, Farshid Najaty Mazgar, 2012. "Symmetric and asymmetric multilevel inverter topologies with reduced switching devices." Electric Power Systems Research, 86: 122–130.

The 3rd international Power Electronics, Drive Systems and Technologies Conference. A New Cascaded Multilevel Inverter with Reduced Number of Switches; [proceedings of the 3rd international Power Electronics, Drive Systems and Technologies Conference,2012] Zahra Bayat, Ebrahim Babaei, 2012.

India IEEE International Conferenceon Power Electronics, 2012. New Cascaded Multilevel Inverter Topology With Reduced Variety of Magnitudes of dc Voltage Sources; [proceedings of 5th India IEEE International Conferenceon Power Electronics] Sepideh Bahravar, Ebrahim Babaei, Seyed Hossein Hosseini.