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# Design of Low Power Double Tail Comparator Using FinFET

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**ABSTRACT**

MOSFETs are widely used in VLSI technology due to minimum short channel effects. As technology advances component dimensions are scaling down. The difficulties in scaling down of conventional MOSFETs can be replaced by using FinFETs. In this paper, delay and average power are calculated for dynamic double tail comparator by using different technologies. Also, a new double tail comparator using FinFET is designed to improve the performance of dynamic double tail comparator. The performance parameters like average power and energy consumption are also alculated for different frequencies using the proposed model. The simulations are performed by frequencies by using SPICE tool and the supply voltage provided for both double tail and proposed comparator are 0.8V.



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## INTRODUCTION

In high speed circuits especially in ADC circuit, comparator plays a very important role. The design of small sized low power comparators with minimum delay is very challenging. In other words, the threshold voltage of the device cannot be scaled down beyond a limit. So the supply voltage should be reduced to meet the requirement of threshold voltage. Reduction in supply voltage is more challenging for the design of high speed comparator. Thus, compensation mechanism for suitable supply voltage can be preferred which in turn will increase the number of transistors. So, area and power requirement will be more for comparators which have supply boosting techniques (Babayan Mashhadi, S. and Reza Lotfi, 2013). Body driven transistors are used for boosting supply voltage. The techniques used for increasing supply voltage are boosting and bootstrapping. But these techniques will create problems related to reliability in ultra deep sub micrometer CMOS technology. The transistors used for boosting supply voltage are body driven transistors which can eliminate the requirements of threshold voltage since these transistors are operated in depletion mode. These transistors can eliminate threshold requirement but the drawback is that the trans-conductance is less compared to gate driven.

The speed of a conventional comparator is less for low voltage operation. Additional large transistors are added to improve the speed of conventional comparator which will increase the area requirement and power. These requirements can be satisfied by adding a few numbers of minimum sized transistors to conventional comparator called as dynamic double tail comparator. In this paper, delay and average power of dynamic double tail comparator is calculated and the result is compared with the conventional comparator using different technologies. The supply voltage provided is given by 0.8V. The main focus of dynamic double tail comparator is to design low power dynamic double tail comparator using FinFET and estimate energy consumption and average power of the proposed comparator by using different frequency.

### *A. Related Work:*

A comparator circuit having modified latch (Goll, B. and H. Zimmermann, 2009) is implemented with 65nm technology which can meet requirements of low supply voltage. The delay can be reduced and it can also support low power with supply voltage requirement as 0.6V. The average power consumption is 128uW. Supply boosting techniques are implemented widely to design high speed comparators. Supply boosting is essential for MOSFETS whose supply voltage is comparable with threshold voltage. 10_bit supply boosted SAR ADC (Mesgarani, A., 2010) is an example for supply boosting technique. Different low voltage design techniques like clock boosting are also used. Newly supply boosted comparators have both clock

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boosting and supply boosting techniques which forms an integral part of ADC. Body driving techniques (Blalock, B.J., 2000) are used for implementing low voltage analog circuits. It is implemented by using class AB power amplifier as an output stage and four quadrant multipliers. This technique can avoid threshold voltage overhead. Signals which are 40 GB/s can be sampled by using a differential comparator (Okaniwa, Y., 2005). It is designed by using 0.11um CMOS technology. Differential comparator mainly consists of sampler, regenerative stage and clocked amplifier. If the feedback gain is high then the reset time will be reduced. So the band width modulation is done by clocked amplifier.

Clocked comparators are the basic building block of ADC especially in flash ADC (Goll, B. and H. Zimmermann, 2007). The requirements of such comparators are small size, low power consumption and high sampling rate. The most effective comparators are sense amplifier based flip flop (Shinkel, D., 2007) having a strong positive feedback which will make fast decisions. The offset value is low due to differential input. Many ADC circuit are having sense amplifiers which is having high input impedance and no static power consumption. Double tail sense amplifiers which are having less stacking of transistors can be operated in low supply voltage range. The double tail provides high current during latching stage and also produce low current for low offset. The advantage is that it provides better isolation between input and output.

***B. Motivation:***

ADCs are the fundamental block in most of the communication systems. Main function of ADC circuit is to convert continuous physical quantity mainly voltage to digital form. The output voltage of ADC circuit is proportional to input voltage. In ADC circuit, the most fundamental device is the comparator circuit. The efficiency of ADC circuit will depend on the speed of comparator. The speed of comparator circuit depends on the supply voltage. In most of circuit, threshold voltage of transistors will depend on supply voltage. The threshold requirements are handled by low supply voltage. In high speed ADCs like flash ADC, high sampling rate and fast switching can be achieved by designing high speed low power comparators. High speed low power comparators can be designed by using supply boosting techniques. So, performance parameters like speed, power, area influence the design of comparators which will affect the efficiency of ADC circuit motivate us to do design low power double tail comparator using FinFET.

The rest of the paper is organized as follows- Section-II describes conventional comparator. Section-III gives the operation of dynamic double tail comparator. Section-IV describes about proposed comparator. Section- V gives the simulation results. Finally, conclusions are drawn in Section- VI.

## II. *Conventional Comparator:*

The basic building block of ADC circuit mainly includes conventional comparator having high input impedance and no static power consumption. The schematic diagram of conventional comparator is shown in fig. 1.

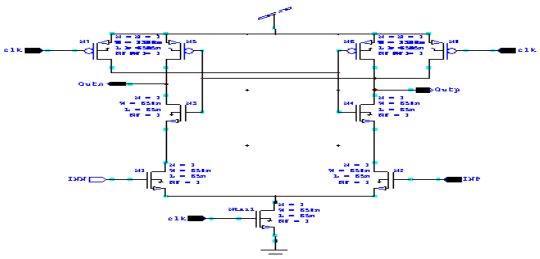

**Fig. 1:** Schematic of conventional comparator.

During Clk=0, transistor $M_{tail}$ is in off state which pull outputs (Outp and Outn) to $V_{DD}$. Also, consider INP > INN causes outp to discharge faster than Outn. In other words, Outn will be at $V_{DD}$ and Outp discharges through ground. If the condition is reversed, the behavior of circuit become vice versa. High input impedance and no static power consumption are the advantages of conventional comparator. The limitation of conventional comparator are supply voltage requirement is high, delay time is high and lower trans-conductance. These limitations can be rectified using double tail comparators.

## III. . *Dynamic Double Tail Comparator:*

The dynamic double tail comparator can be used for low voltage applications. The performance of dynamic double tail comparator is better compared to conventional comparator. The schematic diagram of dynamic double tail comparator is shown in fig. 2.

The purpose of dynamic double tail comparator is to increase the latch regeneration speed. This speed can be improved by adding two control transistors namely $M_{C1}$ and $M_{C2}$ which are cross coupled to each other. When Clk=0, both $M_{tail1}$ and $M_{tail2}$ are in OFF state, making transistors $M_3$ and $M_4$ ON. Thus the outputs $f_n$ and $f_p$ becomes $V_{DD}$. Due to high output,

both transistor $M_{c1}$ and $M_{c2}$ in cutoff region. This will cause both $M_{R1}$ and $M_{R2}$ to reset both the outputs $f_n$ and $f_p$.

When Clk= $V_{DD}$, both $M_{tail}$ and $M_{tail2}$ are in ON state which causes $M_3$ and $M_4$ become turn off. Initially when Clk=1, the voltage at output $f_n$ and $f_p$ are pre-charged to $V_{DD}$ and gradually the output drops at different rates depending on the input voltage. In other words, output voltage drop depends on the input voltages $V_{INN}$ and $V_{INP}$. If $V_{INP} > V_{INN}$ , the voltage drop at $f_n$ is more faster than $f_p$. When $f_n$ continues to fall down, the corresponding PMOS control transistor $M_{c1}$ will be ON which pulls the output $f_p$ to $V_{DD}$. This causes $M_{c2}$ to be in OFF state which will completely discharge $f_n$. In order to avoid static power consumption, below the input transistor $M_1$ and $M_2$ two nMOS switches are connected. The two nMOS switches perform latch operation. When both outputs are pre- Charged to $V_{DD}$, both nMOS switches are closed which will cause the outputs to discharge at varying rates depending on the input voltage. When discharging rate is different, one of the outputs is rising to $V_{DD}$; the other output should be discharged completely. This causes the switch at charging path should be open and switch at discharging path should be closed. Thus the operations of nMOS switches are similar to latch.

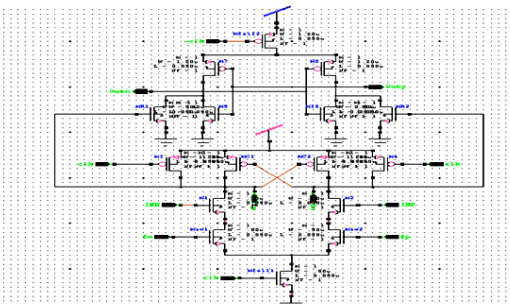

**Fig. 2:** Schematic of dynamic double tail comparator.

IV. ***Dynamic Double Tail Comparator Using Finfet:***

The performance of dynamic double tail comparators can be improved by designing using FinFET. The performance of circuits can be improved by perfect design of FinFET. FinFET is a multigated device which consume very small amount of power. As the device size is reduced, both short channel effect and leakage current can be avoided and this is the advantage of FinFET. Representation of both pFinFET and nFinFET are shown in fig. 3 and fig. 4.

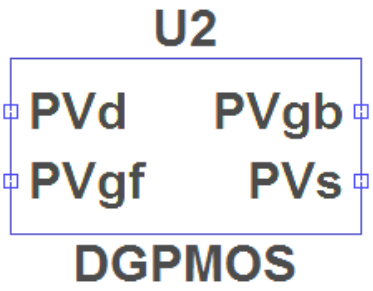


**Fig. 3:** Symbol of pFinFET.

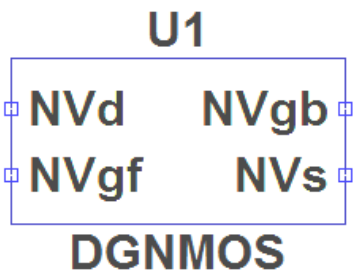


**Fig. 4:** Symbol of nFinFET.

Both pFinFET and nFinFET are modeled in SPICE tool having two gate terminal NVgf and NVgb. Depending upon the purpose of device, different connections can be provided for both gate

terminals. When the gates are shorted together, the power is reduced while if the gates are independent, delay is reduced. The schematic for dynamic double tail comparator using FinFET is shown in fig. 5.

The operation of dynamic double tail comparator using FinFET is same as that of dynamic double tail comparator. If the Clk pulse = 0, it is called as reset phase and when the Clk pulse = $V_{DD}$, it is called as decision making phase. During reset phase, both the outputs are at $V_{DD}$. During decision phase, the outputs starts to drop at different rates based on the input. In dynamic comparator, the Clk pulse will decide whether the circuit will operate in reset phase or in decision making phase. The inputs to the dynamic comparators are mainly INN and INP. When $V_{INP} > V_{INN}$ , the output $f_n$ will drop faster than $f_p$. This causes $f_n$ to discharge completely and $f_p$ to be at $V_{DD}$.

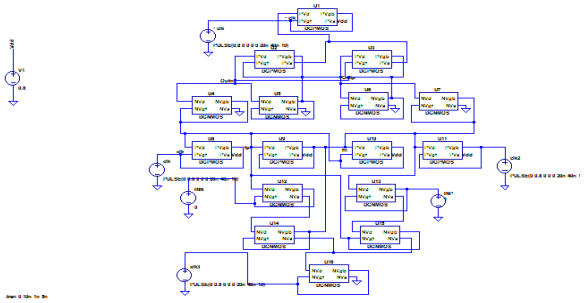

**Fig. 5:** Schematic diagram of dynamic double tail comparator using FinFET.

### *A. Advantages of FinFET:*

FinFET provide excellent control of short channel effects in DSM counterpart. Due to this reason, transistors are more scalable. This will result in smaller transistor length which will increase the intrinsic gain. The leakage current is less compared to MOS devices and the operating voltage requirement is low and provides better speed and low power consumption.

## V. *Simulation Results:*

The circuits for both conventional and dynamic comparator are simulated using different CMOS technologies with supply voltage $V_{DD}$= 0.8V are shown in fig. 6 and fig. 7.

Circuit for double tail comparator using FinFET is simulated using SPICE tool with supply voltage at 0.8V which is shown in fig. 8.

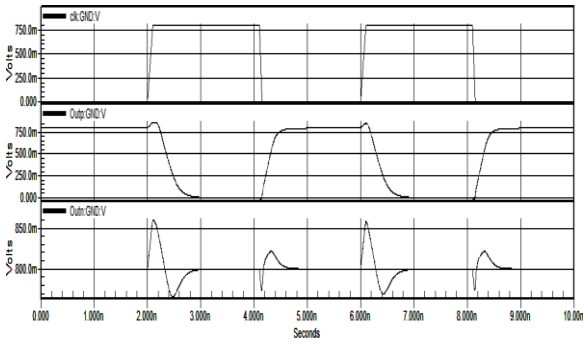


**Fig. 6:** Transient response of conventional comparator for $V_{DD}$ = 0.8V.

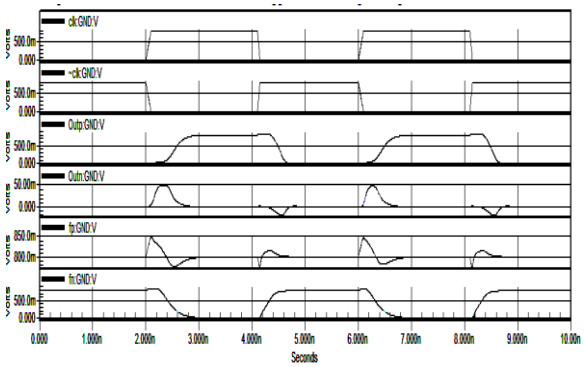


**Fig. 7:** Transient response of dynamic double tail comparator with $V_{DD}$ = 0.8 V.

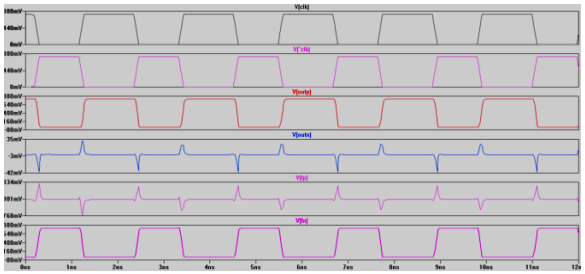

**Fig. 8:** Transient response of double tail comparator using FinFET with $V_{DD}$ = 0.8V.

**Table I:** Delay And Average Power Calculation of Conventional Comparator.

| CMOS TECHNOLOGY | DELAY(S) | AVERAGE POWER (W) |
|---|---|---|
| 180nm | 2.0011n | 0.47mW |
| 130nm | 1.9584n | 0.32mW |
| 65nm | 1.8242n | 0.31mW |

**Table II:** Delay And Average Power Calculation of Dynamic Double Tail Comparator.

| CMOS TECHNOLOGY | DELAY(S) | AVERAGE POWER(W) |
|---|---|---|
| 180nm | 437.4028p | 0.45mW |
| 130nm | 202.4335p | 0.31mW |
| 65nm | 73.1341p | 0.13mW |

**Table III:** Average Power Consumption And Energy For Double Tail Comparator Using FinFET.

| FREQUENCY (Hz) | AVERAGE POWER (W) | ENERGY (J) |
|---|---|---|
| 50MHz | 1.696nW | 0.0256fJ |
| 928MHz | 3.854nW | 0.03469fJ |
| 2.4GHz | 10.087nW | 0.090782fJ |
| 5.875GHz | 17.959nW | 0.16163fJ |

The variation in delay and average power for conventional and for dynamic double tail comparator are estimated by using different CMOS technologies and the results are shown in table I and table II. Average power and energy consumption for dynamic double tail comparator using FinFETare estimated for different frequiencies and the results are shown in table III. From the above table, the inference is that as the technology diminishes, the delay and average power associated with circuit also decreases. Also, as the frequency increases the average power and energy consumption also increases. Compared to both conventional and dynamic comparator, the average power consumed by the proposed comparator is very small.

***Conclusion:***

In this paper, a comprehensive analysis of delay and average power for both conventional comparator and dynamic double tail comparator using different CMOS technologies are calculated. Also, a new comparator circuit using FinFET were designed and implemented. The performance parameters like average power and energy consumption of the proposed circuit are estimated using different frequencies and comparison of proposed comparator with both conventional comparator and dynamic comparator are also considered.

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