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Performance Analysis of Anurupye Vedic Multiplier in FFT Processor

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ABSTRACT

A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. This paper presents the performance analysis of vedic multiplier such as Urdhva Tiryakbhyam and Anurupye. Since high speed 8-point Vedic multiplier architecture is quite different from the conventional method of multiplication like add and shift. The most significant aspect is that, the developed Anurupye multiplier architecture is based on proportionality, i.e Select a theoretical base which is common to both numbers and then take a proportional base to the theoretical base as acting as the working base. So the design complexity gets reduced for inputs of larger number of bits and modularity gets increased. The proposed Vedic multiplier is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language), synthesized and simulated using vivado 14.1. Finally the Anurupye results are compared with Urdhava Tiryakbhyam and array multiplier to show the significant improvement in its efficiency in terms of path delay (speed) and power. The high speed processor requires high speed multipliers and the Vedic Multiplication technique is very much suitable for this purpose

INTRODUCTION

The ancient system of Vedic Mathematics was rediscovered from the Indian Sanskrit texts known as the Vedas, between 1911 and 1918 by Sri Bharati Krishna Tirthaji (1884-1960) from the Atharva Vedas. According to his research all of mathematics is based on sixteen Sutras, or word-formulas (Narchi, P., 2011). These formulae describe the way the mind naturally works and are therefore a great help in directing the student to the appropriate method of solution. In the Vedic system difficult problems or huge sums can often be solved immediately by the Vedic method. These striking and beautiful methods are just a part of a complete system of mathematics which is far more systematic than the modern system. Vedic Mathematics manifests the coherent and unified structure of mathematics and the methods are complementary, direct and easy (Vaidya, S., D. Dandekar, 2010; Kumar, A., 2010). An awareness of Vedic mathematics can be effectively increased if it is included in engineering education. In future, all the major universities may setup appropriate research centers to promote research works in Vedic mathematics. The power of Vedic mathematics is not only confined to its simplicity, regularity, but also it is logical. Its high degree of eminence is attributed to the aforementioned facts. 'Vedic mathematics' logics and steps can be directly applied to problems involving trigonometric functions, plane and sphere geometry, conics, differential calculus, integral calculus and applied mathematics of various kind. The advantage of Vedic mathematics lies in the fact that it simplifies the complicated looking calculations in conventional mathematics to a simple one in a much faster and efficient manner. This attribute to the fact that, the Vedic formulae are claimed to be based on the "natural principles on which the human mind works". Hence this presents some effective algorithms which can be applied to various branches of engineering. In this paper

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FFT processor design using Vedic multiplier with Anurupye sutra which denotes "If one is in ratio, the other is zero operation" is implemented. Conventional mathematics is an integral part of engineering education. Since most engineering system designs are based on various mathematical approaches. All the leading manufacturers of microprocessors have developed their architectures to be suitable for conventional binary arithmetic methods. The need for faster processing speed is continuously driving major improvements in processor technologies, as well as the search for new algorithms. The Vedic mathematics approach is totally different and considered very close to the way a human mind works. A large amount of work has so far been done in understanding various methodologies (sutras) (Kumar, G.G., V. Charishma, 2012; Kerur, S.S., 2014)] . Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application (Agarwal, J., 2010). The results are compared in terms of power, delay and area. Fast Fourier Transform (FFT) design methodology using Vedic mathematics algorithms such as Anurupye and Urdhava Tiryakbhyam provides a fast and reliable approach to compute the N-point and the performance is analysed.

II. Vedic Mathematics:

Multiplication is an important function in arithmetic operations. Multiply and Accumulate (MAC) is one of the frequently used Computation- Intensive Arithmetic Functions (CIAF) that are implemented in many Digital Signal Processing (DSP) applications such as convolution operation, filtering, Fast Fourier Transform (FFT) and in microprocessors in its arithmetic and logic unit(ALU). It can be implemented using many algorithms such as array multiplication, booth multiplication, carry save adder, and Wallace tree algorithms used for myriads (Raman, A., 2010). As a processor spends considerable amount of time in performing multiplication operation of numbers, an improvement in multiplication speed can greatly improve by the system performance (Bhongade, R.K., 2014).

2.1. Urdhava Tiryakbhyam:

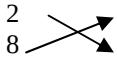
Urdhava Tiryakbhyam is a Sanskrit word which means vertically crosswise in English. The method is a general multiplication formula applicable to all cases of multiplication. It is based on a novel & rudimentary concept through which all kind of partial products are generated concurrently.

2.2. Anurupye (Shunyamanyat) Sutra:

The upa-Sutra Anurupye means 'proportionality'. Three-digit multiplication (e.g. 532 x 438) is based on this sutra is explained below.

Step 1 & 2:

Here 100 as the theoretical base and 100*5=500 as the working base.



```
5   3   2        +32
4   3   8        -62
-----------------------------------------
4   7   0        -1984
```

Step 3:

Since 100 is the theoretical base so RHS has two digits (84). Carry over the (-19) to LHS.

As per sutra says "Proportionality" LHS is multiplied by 5 to get the working base from the theoretical base.

470*5 =2350-19=2331

Step 4:

Since RHS is still a Negative number, to make it positive it is complimented with its theoretical base

100-84=16

Subtract 1 extra from LHS for coming out of compliment

2331-1=2330

Answer is 532*438=233016

III. Implementation of FFT Processor Using Vedic Multiplier:

The 8 bit Vedic multiplier using Urdhava Tiryakbhyam and Anurupye sutra is designed in VHDL Logic Synthesis and Simulation is done in vivado 14.1. This paper analyze the 8-point multiplications, say A= A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0 and B= B_7 B_6 $B_5$$B_4$ B_3 B_2 $B_1$$B_0$. The output line for the multiplication result will be of 16 bits as – $S_{15}$$S_{14}$$S_{13}$ S_{12} S_{11} S_{10} S_9 S_8 S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0. Divide A and B into two parts, the 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The

16 bit product can be written as P = A x B = (AH-AL) x (BH-BL) = AH x BH + (AH x BL + AL x BH) + AL x BL Using the fundamental of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block can perform the multiplication. The outputs of 4x4 bit multipliers are added accordingly to obtain the final product.

3.1. 8-point FFT module:

In the DSP Processor, a large amount of work has been devoted to reducing the computation time of a DFT (Baas, B.M., 1999). This has led to efficient algorithms which are known as the Fast Fourier Transform (FFT) algorithms. The N-point discrete Fast Fourier Transform (DFT) is defined in equation (1).

$$X(k) = \sum_{n=0}^{N-1} x[n] e^{-j\left(\frac{2\pi}{N}\right)nk} \quad (1)$$

X(k) is the k-th harmonic and x(n) is the n-th input sample. Direct DFT calculation requires a computational complexity of O(N2). The flow graph of complete Decimation in Time (DIT) decomposition of 8-point DFT computation is represented in Fig.1 (Vaithiyanathan, G., 2013).

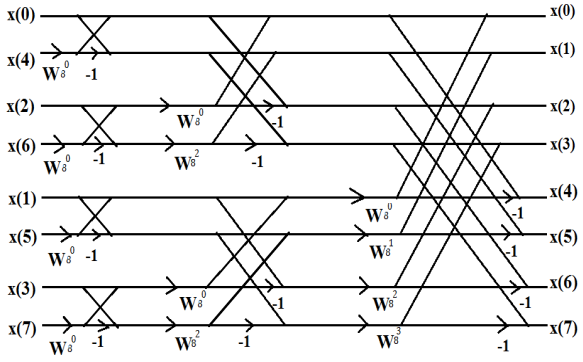


Fig. 1: 8-Point DIT in FFT Algorithm.

RESULT AND DISCUSSION

In this paper, Vedic Multiplier based design of 8 point FFT using Anurupye sutra has been implemented and its performance is compared with Urdhava Tiryakbhyam. RTL View is a Register Transfer Level graphical representation of the design. It is represented in terms of macro blocks, such as adders, multipliers, and registers. Standard combinatorial logic is mapped onto logic gates, such as AND, NAND, and OR.

The RTL view of 8×8 bit Vedic multiplier using Urdhava and Anurupye is shown in Fig.2 and 3.

The simulated response for 8×8 bit Urdhava and Anurupye is shown in Fig 4 and 5.

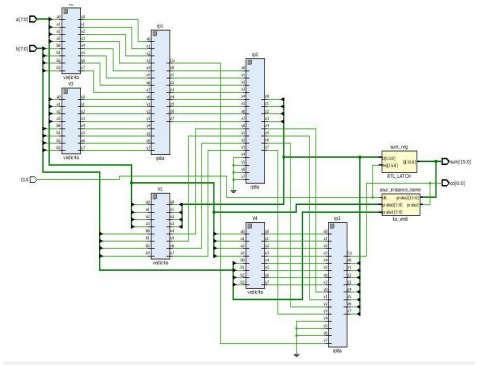


Fig. 2: RTL View of 8×8 Vedic multiplier (urdhava).

FFT processor is implemented by using both Urdhava and Anurupye algorithm based Vedic Multiplier and compared with Array Multiplier. The simulated response is analysed and the validating parameters such as power, number of gates and delay are compared. The RTL view of 8 point Array FFT and FFT using Urdhava and Anurupye is shown in Fig 6, Fig 7 and Fig 8.

The simulated response for FFT based Urdhava and Anurupye is shown in Fig 9 and 10.

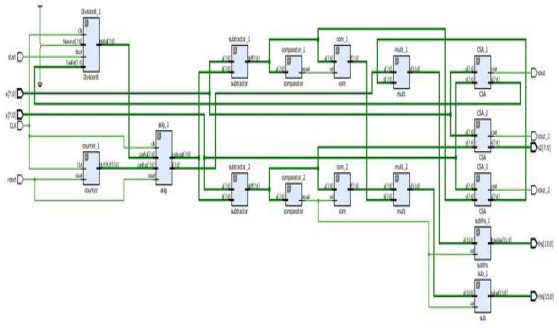


Fig. 3: RTL View of 8×8 Vedic multiplier (Anurupye).

Fig. 4: Simulated Response for 8×8 bit Urdhava.

Fig. 5: Simulated Response for 8×8 bit Anurupye.

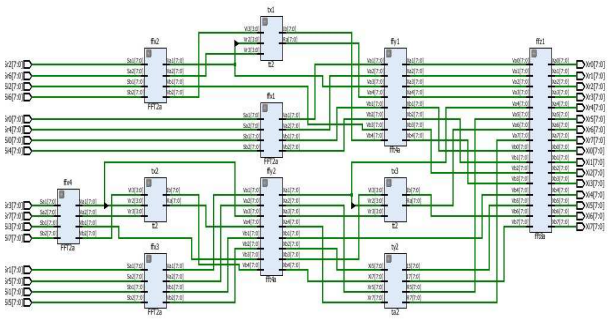


Fig. 6: RTL View of Array FFT.

From the Table 1 the performance of array multiplier is compared with the performance of Vedic multipliers implemented in two sutras i.e Urdhava Tiryakbhyam and Anurupye. It shows that the Anurupye sutra based vedic multiplier gives optimum performance than Urdhava by reducing power and delay.

From the Table 2 the performance of FFT processor based on array multiplier is compared with the performance of Vedic multipliers implemented in two sutras i.e UrdhavaTiryakbhyam and Anurupye. It shows that the Anurupye sutra based vedic multiplier in FFT processor gives more efficient performance than Urdhava by reducing power and delay and number of gates.

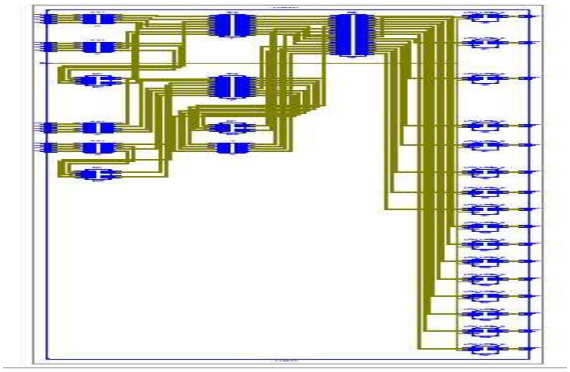


Fig.7: RTL View of FFT(Urdhava).

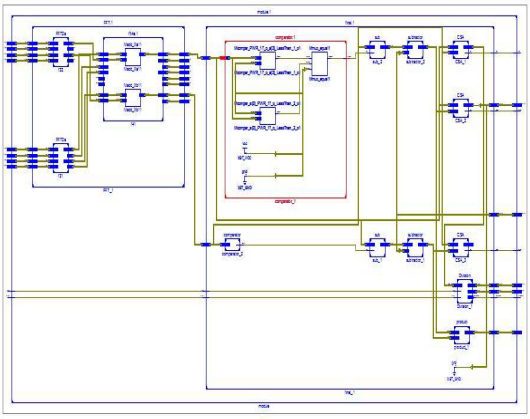


Fig. 8: RTL View of FFT(Anurupye).

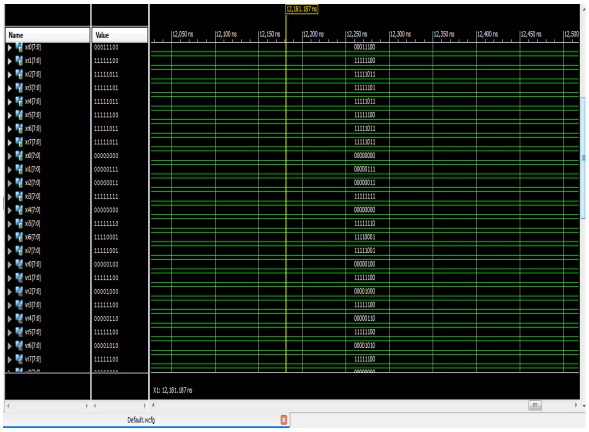


Fig. 9: Simulated Outputs of FFT(Urdhava).

V. Conclusion:

Minimizing power consumption for digital systems is a vital problem and it involves optimization at all levels of the design. Multiplier design based on Vedic Mathematics is one of the suitable solution for this problem and it gives fast and low power output. However, the optimization may be achieved at the expense of area, power dissipation, propagation delay and accuracy of the digital system. So efforts should be made to decrease the number of multipliers and thereby increase their speed. In this paper, A high speed complex multiplier of FFT Processor design using Vedic multiplier with Anurupye sutra is implemented and the performance is analyzed. This sutra is applicable to all cases of multiplication. From the comparison table, Anurupye Vedic multiplier on FFT is made efficient than Urdhava Tiryakbhyam sutra by more reduction in power and delay and number of gates.

Fig. 10: Simulated response of FFT based Anurupye algorithm.

Table 1: Multipliers performance.

PARAMETER	ARRAY MULTIPLIER	VEDIC MULTIPLIER	
		Urdhava Tiryakbhyam sutra	Anurupye sutra
DELAY	22.035ns	23ns	20.546ns
POWER	56mw	52mw	34mw

Table 2: FFT processor performance.

PARAMETER	ARRAY MULTIPLIER	VEDIC MULTIPLIER	
		Urdhava Tiryakbhyam sutra	Anurupye sutra
NO. OF SLICES	3337	786	674
DELAY	25.6ns	21.2ns	17ns
POWER	96.92mw	82.73mw	64mw

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