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Reliable High Performance (RHP) SRAM Cell for Write/Read Operation

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ABSTRACT

Background: Static random access memory (SRAM) is critical component of cache due to its high speed and compatibility with standard processor. The power dissipation in SRAM cell has become an important consideration due to increased demand of high speed and portable battery operated devices. Although, the conventional 6T SRAM cell has large storage capacity but it suffers from large power consumption (dynamic and static) and degraded performance/reliability. Therefore, design of reliable power efficient high performance SRAM cell becomes a necessity. **Objective:** This paper presents a reliable high-performance (RHP) power efficient SRAM cell for read/write operations. **Results:** The simulated results indicate that read and write power consumption of RHP cell are 51% and 78.48% lower than the 6T which confirm the desire of this design. **Conclusion:** The RHP cell is analysed under different criteria such as power consumption, write ability, speed and read stability. A new write technique is projected to reduce the charging/discharging activity on the respective bit lines.

INTRODUCTION

The demand for the portable devices and battery embedded systems continuously increases, the power consumption has become a main consideration in the microprocessor and system designs. In recent VLSI system, SRAM cell area is larger on the chip. Due to demand of green technology, it is great challenge to the researchers to limit the power dissipation in the latest processor. Most of the low power design SRAMS are based on decreasing the voltage swing level and capacitance. Word line, bit lines and data lines the highest value of the capacitive parts in the memory. Low-power SRAM techniques are mostly reducing the read power only. (Grossar, E., *et al*., 2006, Sil, A *et al*., 2007, Sayeed A.Badrudduza *et al*., 2008, and Prabhu, C.M.R *et al*., 2010) but normally power dissipation during write operation is higher than read operation (Kanda, K *et al*., 2004, Yen-Jen Chang *et al*., 2004, Aly, R.E., 2007and Prabhu, C.M.R *et al*, 2010). Because of the recent technology when the researchers are reduced the future size, the power consumption is also reduced but stability and access time are degraded. To overcome the stability problem in 6T cell, many SRAM cells are proposed (Abhijit Sil *et al*., 2007, Liu, Z *et al*, 2008, Islam, A *et al*, 2012 and Prabhu, C.M.R *et al*, 2010).

The proposed reliable high-performance (RHP) cells uses separate circuit for read and write operations to improve the stability and performance. A new RHP cell contains two extra nMOS transistor at the feedback link of the two inverters. The logic level at bit lines (BL and BLB) are controlled the switching behaviour of the feedback path transistors. Both feedback transistors to break the link between the inverters before any write operation. Entire simulated results were obtained in 65nm CMOS technology using SPICE simulation and advance BSIM 4 model (Microwind3 tool). The rest of the paper is structured as follows. The RHP SRAM cell is explained in section 2. In Section 3, simulated results and comparison are discussed. Section 4 concludes the paper.

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Proposed Reliable High-Performance Sram Cell:

Figure 1 shows the architecture of the proposed RHP SRAM cell. The RHP cell has two isolated circuits, namely, read and write circuits to improve the stability of the cell so that the stored data in the cell remains intact during read/hold operation. The write circuit contains two cross coupled inverters as in the conventional 6T cell except that two transistors N6 and N7 are added in feedback paths. The switching behavior of these two feedback transistors are controlled by the voltage level at BL and BLB respectively. During write operations, one of the feedback paths is broken so that data can be flipped faster at the respective nodes without consuming considerable dynamic power. In the proposed RHP SRAM cell, no extra signal is used as in other cells proposed in the literature (Yen-Jen Chang *et al*., 2004 and Aly, R.E., 2007). In the cell, read operation is performed using transistors N7 and N2. The detail operation of RHP cell is;

During read operation, BL and BLB are set to V_{DD} which turns ON the feedback transistors so that latch property of the cell is restored. Depending upon the voltage at the Q2, read bitline RBL either discharges or maintains its precharged value V_{DD}. If Q2=V_{DD}, then precharge RBL will discharge through two series connected ON transistors N7 (RWL=V_{DD}) and N2. This is equivalent to read 0 operation. When Q2=0V, transistor N2 turns off and does not allow RBL to discharge. This is read 1 operation. The cell node is disconnected from the read bit line RBL due to off transistor N7 transistor during standby/write mode which restricts the leakage current in the cell.

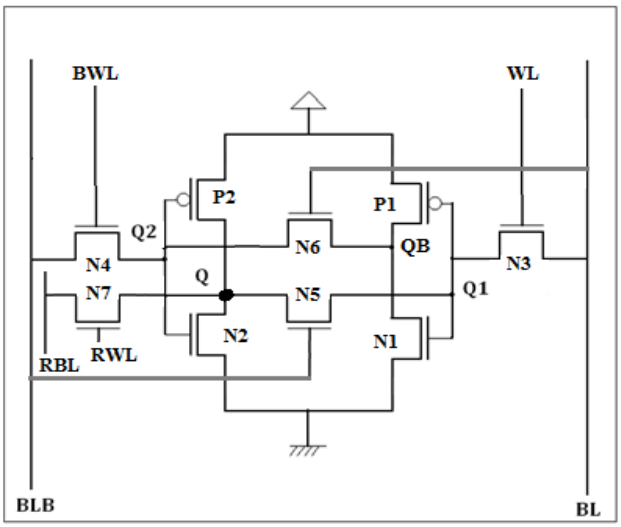

Fig. 1: RHP SRAM cell

During write operation, RWL=0 so that read circuit is completely isolated from write circuit which restricts the leakage current of the read circuit. To write '1' at node Q the bitline has to be set at BL = 1 and BLB (bit line bar) =0. Transistor N6 is turn ON, while transistors N5 and N3 are turned OFF. Once WL is high, the access transistor N3 is turned ON by WL and the access transistor N4 is turned OFF by BWL. Therefore, BLB is disconnected from the node Q2 as shown in Fig. 2(a). The high input at the inverter, formed by P1 and N1, flips the data at Q high. Due to the feedback mechanism, the proposed RHP SRAM cell dissipates lower power than the 6T SRAM cell during write operations.

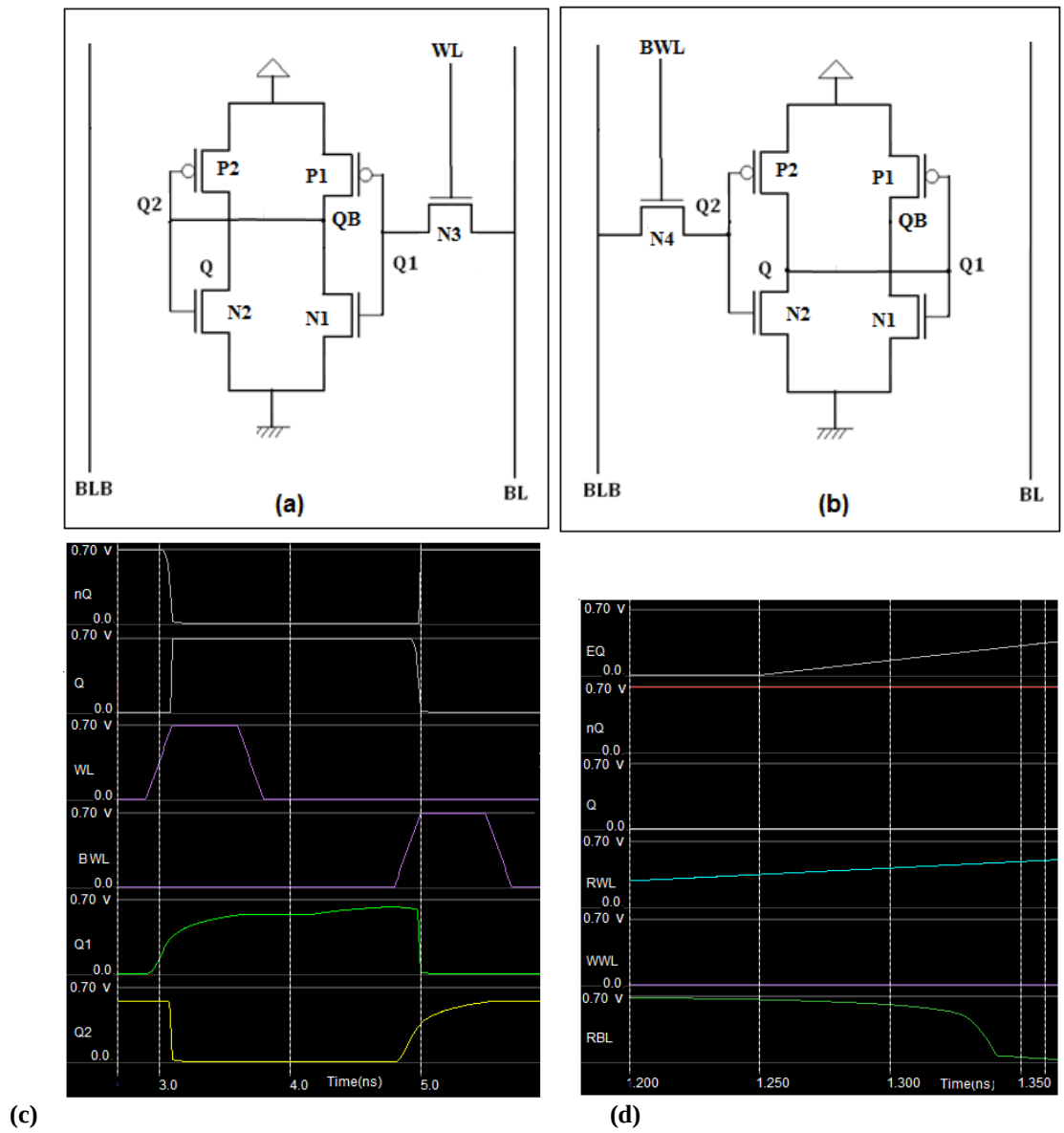

Fig. 2: (a)RHP Cell during :(a) write '1' mode(b) write '0' mode and Output waveform :(c) for two consequent write operation (d) for read operation

To write '0' at node Q the bit lines have been set at BLB = 1 and BL=0. Now transistor N5 turns ON, and transistors N6/N3 turned OFF. Once BWL is 'high', the access transistor N4 is turned ON and the access transistor N3 is turned OFF by WL (WL and BWL are complementary of each other). BL is disconnected from the node Q1 as shown in Fig. 2(b). The data is transferred from BLB to Q2 using N4 which drives inv.2, P2 and N2, to flip low data at Q. Now, again both BL and BLB are precharged while transistor N6 is turned ON to recouple the two inverters. Due to the reconnection of the feedback link, the proposed cell is able to intact the stored data. The waveforms during write 1 and write 0 operations are shown in Figure 2(c) and 2(d) respectively.

RESULT AND DISCUSSION

The proposed RHP cell is simulated with the help of DSCH3 and Microwind3 in terms of speed, power consumption, SNM and other performance metrics to analyze the characteristics of the cell. The simulations are carried out at the layout level for 65nm CMOS technology using advanced BSIM4 model with V_{DD}=0.7V. The two feedback transistors in the write circuit allows the data to be directly used as an input of the respective inverter which flips the logic at node Q faster (Table 2) without allowing BL or BLB to discharge. The lower discharging activity at the bit line saves considerable dynamic power compared to the conventional 6T cell and cell proposed in ref.[6] (Table1). We have observed the write power saving is about 78.48% compared to the 6T

cell. There is also power reduction for transition 0→1, when compared with 7T SRAM cell about 82.44%. This proves that, the proposed cell power efficient during the write operation.

Table 1: Write power

		WRITE OPERATION			
		0→0	0→1	1→0	1→1
Power (µW)	6T	0.016	4.938	4.944	0.017
	7T[6]	0.004	5.073	0.987	0.018
	RPH	0.004	0.892	0.891	0.004

Table 2: Access Time

		Write Access Time		Read Access Time	
		0 → 1	1 → 0	Read'0'	Read'1'
Delay (ps)	6T	128	128	80	80
	7T[6]	136	62	80	91
	RHP	60	60	81	15

Table 3: Temperature on Standby Power

Temperature	Standby Power(nW)	
	Conv.6T	RHP Cell
27°C	16	4
50°C	34	11
75°C	51	20
100°C	92	42
125°C	155	74
137°C	192	95

Since the read '0' operation in the proposed cell is similar to the 6T cell, so that the RHP cell maintains same read '0' delay as shown in Table 2. For read '1' operation, N2 turns OFF. Since RBL and node Q at '1', RBL does not discharge which accelerates the read operation. Due to forbidden discharging at RBL during read 1 operation saves average read power about 51% compared to the other cells (Figure 3).

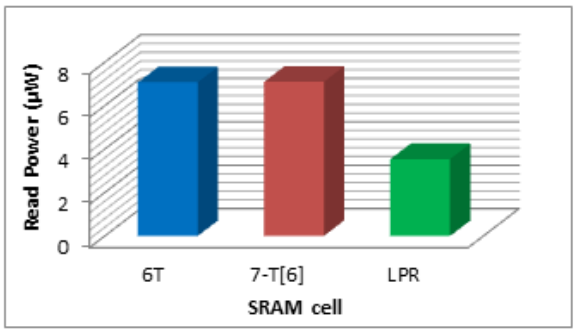

Fig. 3: Read power consumption

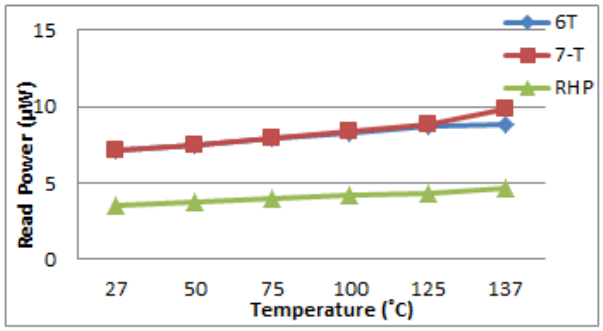

Fig. 4: Read power with Temperature

As temperature increases from 27° C to 137 °C, the standby and read power consumption is lower than the other cells as given in Table 3 and shown in Figure 4. This lower power consumption with temperature is due to restricted leakage current in the cell because read and write ports are isolated from each other. The graphical butterfly curve is used to measure the SNM (Prabhu, C.M.R *et al*., 2010 and Seevinck, E *et al*., 1987). Fig. 5 shows the SNM of the 6T cell and RHP cell. The SNM of the RHP cell is 265mV which is 2.4x higher than the 6T SRAM cell (75mV) due to two isolated read and write circuits. The larger SNM provides better read stability in the proposed RHP cell which avoids any loss of data during read operation. Fig.6 reflects that the percentage change in SNM is only 15% fall as temperature varies from -20°C to 137°C. This lower fall in SNM is due to lower leakage current in the proposed cell. Fig.7 shows a slight variation in read SNM with change in threshold voltage of transistor N7 due to low leakage current in the cell through the read access transistor and read bit line RBL.

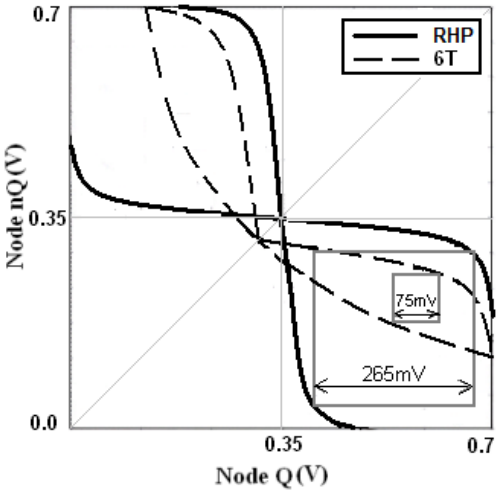

Fig. 5: Graphical representation of SNM

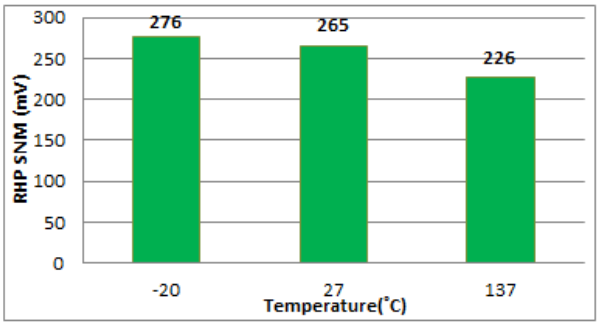

Fig. 6: SNM of RHP with temperature

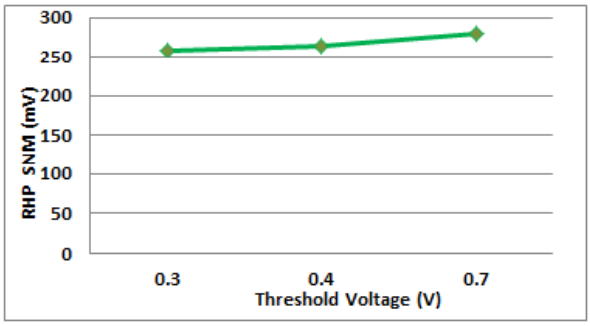

Fig. 7: RHP SNM with Threshold voltage

Conclusion:

The proposed RHP SRAM cell flips data faster at the storage nodes and consumes lower power during write operation due to use to two feedback transistors. The feedback transistor applies the complement of the data to be written in the cell directly as an input of the inverter which flips the storage data without waiting the bit line to discharge. The reduced discharging activity at the write bit line saves dynamic power in the cell. The isolated read and write ports in the cell enhances the read stability as well as restrict the leakage current in the cell which results in lower power consumption with temperature during hold mode and read operation. The increased SNM of the cell reduces the probability of losing data during read/hold mode. The simulated results indicate that read and write power consumption of RHP cell are 51% and 78.48% lower than the 6T cell. The proposed RHP SRAM cell avoids use of any extra signal which leads in reduction of hardware burden.

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