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Fast Low Power (FLP) SOI SRAM Cell for Write/Read Operation

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ABSTRACT

Background: Memories with low power and high speed are playing vital role in the entire VLSI industry mostly in mobile devices and battery powered portable electronic system. The power dissipation and performance are important consideration for System on chip designers when finding the balance between the size, its performance and the overall power consumption. Therefore fast low power SOI SRAM cell becomes a necessity. **Objective:** In this paper, we propose a fast low power SOI SRAM cell for read/write operations. The objectives of this paper are to reduce the power and improve the performance during the read/write operation. **Results:** The simulated results indicate that read and write power dissipation of FLP SOI cell are 50% and 81.97% lower than the 6T which confirm the desire of this design. **Conclusion:** The FLP SOI cell is analysed in terms of power consumption, write ability, speed and read stability. A new write technique is projected to reduce the charging/discharging activity on the respective bit lines.

INTRODUCTION

Embedded memory is an important requirement in modern system on chip (SoC) designs. Power dissipated by embedded SRAM caches plays an important role in the overall power consumption of the chip because embedded SRAM generally consumes a considerable portion of the total power. Thus the SRAM power consumption is an important consideration for SoC designers when finding the balance between the cache size, performance and the overall power consumption. The power consumption in the SRAM cell is generally categorized as either static power consumption, or dynamic power consumption. To accomplish fast and low power consumption, the feature size of CMOS devices has been dramatically scaled to smaller dimensions. As the technology shrinks, leakage current becomes a major source for overall power consumption of the chip. Therefore, currently, Silicon On Insulator (SOI) technology is largely used in SRAM designs. Its performance is merited with low power dissipation, low noise, high rejection to radiation, and no latch-up effect in contrast with conventional CMOS cell (Jacob, J.B *et al*., 1998, Francis, P *et al*., 1992, and Bruel, M, 1995). Thus, SRAM cell's performance can be enhanced based on SOI technology. Researchers have proposed various methods on architecture level as well as process level to reduce the power dissipation in SRAM cell (Grossar, E., *et al*., 2006, Sil, A *et al*., 2007, Sayeed A.Badrudduza *et al*., 2008, Kanda, K *et al*., 2004, Yen-Jen Chang *et al*., 2004 and Aly, R.E., 2007 and Prabhu, C.M.R et al, 2010). These methods were developed to improve the read/write stability as well (Abhijit Sil *et al*., 2007, Liu, Z *et al*, 2008, Islam, A *et al*, 2012 and Prabhu, C.M.R. *et al*., 2014)

In this paper, we have proposed a fast low power (FLP) SOI SRAM cell with two circuits (write /read) to increase the access time and reduce the power dissipation. During write pattern, the latch property is cut-off to flip the data on the storage nodes faster by feedback transistors. Entire simulated results were obtained in 0.12μm SOI CMOS technology using SPICE simulation and advance BSIM 4 model (Microwind3 tool). The

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rest of the paper is structured as follows. The FLP SOI SRAM cell is explained in section 2. In Section 3, simulated results and comparison are discussed. Section 4 concludes the paper.

Proposed Fast Low Power Soi Sram Cell:

Figure 1 shows the schematic of the FLP SOI SRAM cell. The FLP SOI SRAM cell has two isolated circuit for read operation and write operation. Due to these two circuits, the earlier stored data remains stable in the cell during write operation. The write circuit contains two inverters inverter1 (P1 & N1) and inverter2 (P2 & N2). The transistors N7 and N8 are controlled by bit lines (BL/BLB) logic level. During write operations the feedback path between two inverters is separating by feedback path transistors N5/N6. The logic level at write signal (W1 and W2) are controlled the switching behaviour of the feedback path transistors N5/N6. The FLP cell operation detail is: During the read mode W1 and W2 are set to V_{DD} which turns ON the feedback transistors and latch property of the cell is restored. Two transistors (N8 and N2) are used to perform the read mode. The cell node is disconnected from the read bit line RBL using N9 transistor during standby/write mode.

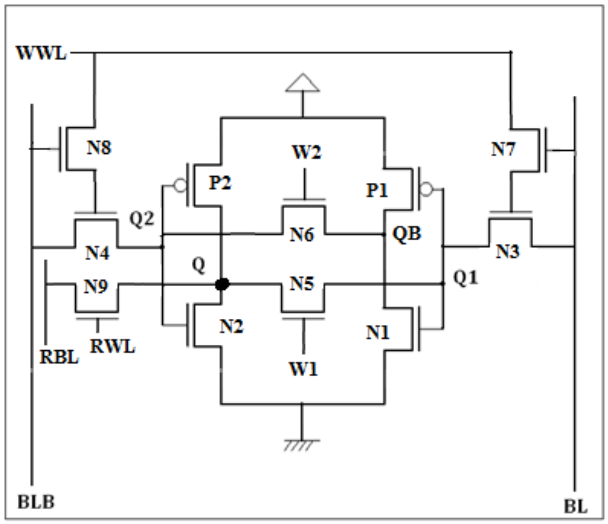

Fig. 1: FLP SOI SRAM cell

During write operation, RWL=0 and read circuit completely disconnected. To write '1' at node Q the bit line has to be set at BL = 1. BLB (bit line bar) carries 0; transistor N6 is turn ON by W2, while transistors N5 is turn OFF by W1 and N4 turned OFF by logic level at BLB. Once WWL is high, the access transistor N3 is turned ON and the access transistor N4 is turned OFF. Therefore, BLB is disconnected from the node Q2 as shown in Fig. 2(a). The data is transferred from BL to Q1 using N3 which drives inv.1, P1 and N1, to change QB which equals Q2. Then, the transistor N5 is turned ON by W1 to recouple the two inverters. Due to this feedback mechanism, the proposed FLP SOI SRAM cell dissipates lower power and faster response than the 6T SRAM during write operation.

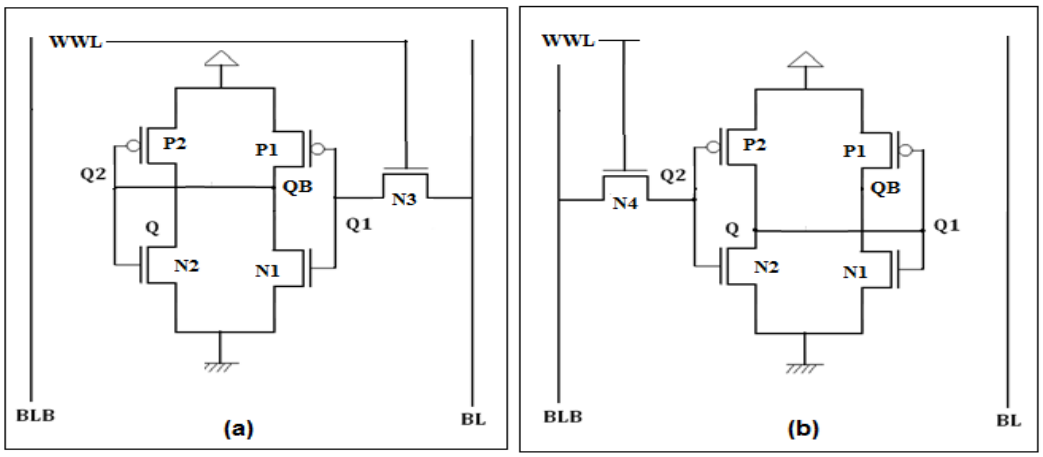

Fig. 2: (a)FLP SOI SRAM Cell during :(a) write '1' mode(b) write '0' mode

To write '0' at node Q the bit line has to be set at BLB = 1. BL (bit line) carries 0; transistors N5 is turn ON by W1, while transistor N6 is turn on by W2 and N3 is turned OFF by BL. Once WWL is '1', the access transistor N4 is turned ON and the access transistor N3 is turned OFF. BL is disconnected from the node Q1 as shown in Fig. 2(b). The data is transferred from BLB to Q2 using N4 which drives inv.2, P2 and N2, to change Q which equals Q1. Then, the transistor N6 is turned ON by W2 to recouple the two inverters. Due to the reconnection of the feedback link, the proposed cell is stably store the new data. A read operation, (RWL = high, WL/BWL = 0); two transistors (N9 and N2) are used to perform the read mode.

RESULT AND DISCUSSION

The proposed FLP SOI cell are simulated in terms of speed, power consumption, SNM and other performance metrics to measure characteristics of typical SRAM cell with help of DSCH3 and Microwind3. The simulations are carried out on the layout level for 0.12µm SOI CMOS technology using advanced BSIM4 model with V_{DD}=1.2V. Since the FLP SOI SRAM cell has an extra two feedback link transistors to couple or decouple the link between the inverters, the storage node data is flipped easily. The write power consumption for other published cell is given in Table1. The proposed FLP SOI cell consumes lower power than the other cell due to forbidden discharging activity at the respective bit-lines. We have observed the write power saving is about 82%. There is also power reduction for transition 0→1, when compared with 7T SOI SRAM cell about 82.46%.Which proves that, the proposed cell power efficient during the write operation.

Table 1: Write power and write access Time

		WRITE OPERATION			
		0→0	0→1	1→0	1→1
Power (µW)	6T SOI	0.016	4.938	4.944	0.016
	7TSOI[2]	0.004	0.987	5.073	0.017
	FLP SOI	0.004	0.889	0.892	0.004
Access Time (ps)	6T SOI	-	128	128	-
	7TSOI[2]	-	62	136	-
	FLP SOI	-	60	60	

Table 2: Read Access Time

		READ OPERATION	
		Read '0'	Read '1'
Access Time (ps)	6TSOI	80	80
	7TSOI[2]	80	91
	FLP SOI	81	15

During read '0' operation, transistor N2 turned ON; two transistors (N9 and N2) are used to perform the read mode. Since the read '0' operation is similar to the 6T SOI SRAM cell, so that the FLP SOI cell maintains same read '0' delay as shown in Table 2. For read '1' operation, N2 turns OFF. Since RBL and node Q at '1', read bit line does not discharge which results in considerable power saving in Fig. 3. Due to lower $V_{discharge}$ voltage, the average read power is reduced to 50% compared to the other cells (Fig.3).

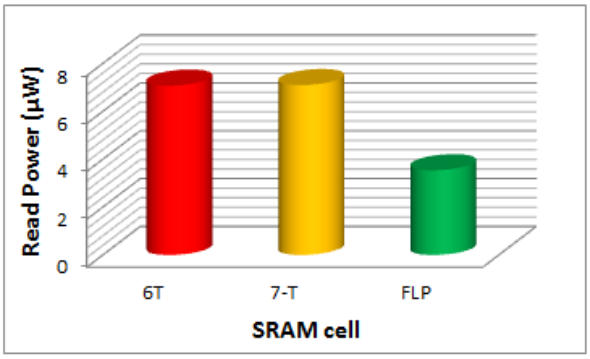

Fig. 3: Read power

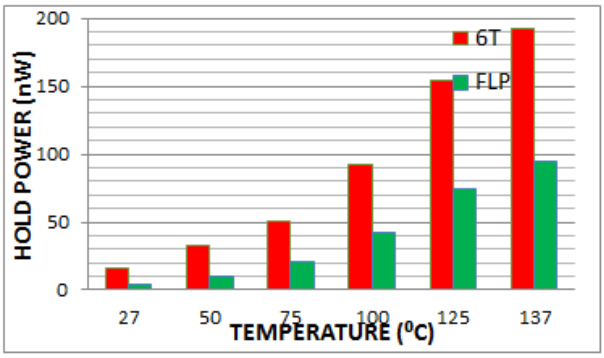

Fig. 4: Hold power with Temperature

As temperature increases from 27° C to 137 °C, the FLP SOI cell standby mode as well as read mode power consumption is lower compared to other cells as shown in Fig. 4 and Fig. 5. The graphical butterfly curve is used to measure the SNM (Prabhu, C.M.R et al., 2014 and Seevinck, E et al., 1987). Fig. 6 shows the SNM of the 6T SOI cell and FLP SOI cell. The SNM of the FLP SOI cell is 294mV which is 2.54x higher than the 6T SOI SRAM cell (83mV) due to two separate circuits. Fig.7 shows the SNM percentage is only decrease (15%) as temperature varies from -20°C to 137°C. Fig.8 shows the slight variation in read SNM with different

threshold voltage of transistor N9. Due to low leakage current in the cell, the read SNM shows a slight variation with Vth .

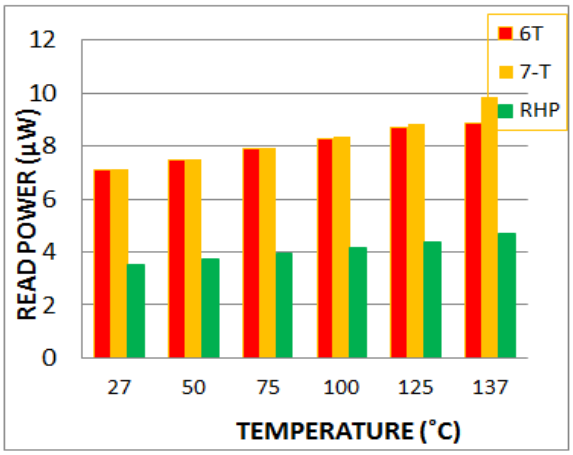

Fig. 5: Read Power with Temperature

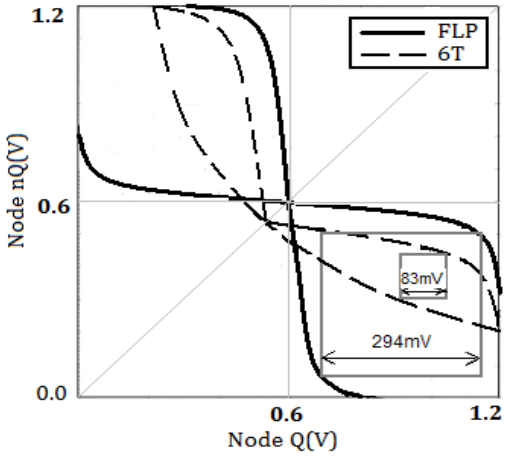

Fig. 6: Graphical representation of SNM

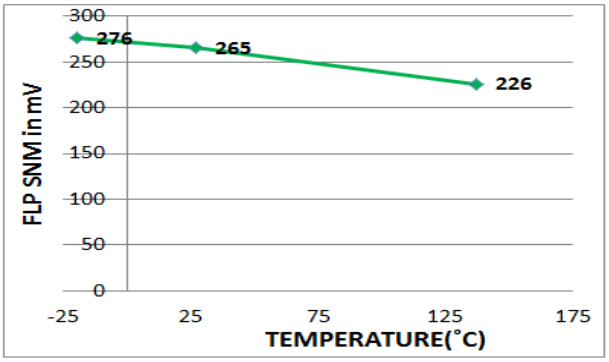

Fig. 7: SNM of FLP with temperature

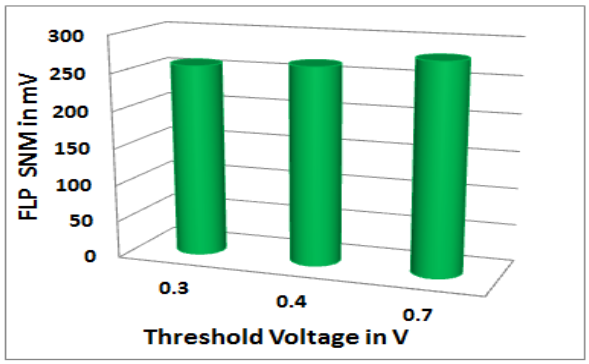

Fig. 8: FLP SOI SNM with Threshold voltage

Conclusion:

In this paper, a fast low power (FLP) SOI SRAM cell is proposed. The write circuit of the FLP SOI cell is performed operation by decoupling feed-back link of the two inverters. The reduced discharging activity at the write bit line saves dynamic power in the cell. The isolated read and write ports in the cell enhances the read stability as well as restrict the leakage current in the cell which results in lower power consumption with temperature during hold mode and read operation. The proposed technique prevents any single bit-lines from being discharge during write mode and thus reduces the power dissipation. The simulated results indicate that read and write power consumption of FLP SOI cell are 50% and 81.97% lower than the 6T SOI cell which confirm the desire of this design. Due to isolation of stored data from bit lines during read operation, the SNM of the proposed FLP SOI cell is 2.54x higher than the 6T SOI cell.

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