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A New Method for Simulation and Modeling of Universal Power Quality Conditioning System

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Abstract: Power quality problems have received a great attention nowadays because of their economical impacts on both utilities and customers. The current harmonics is the most common problem of power quality, while voltage sags is the most severe. Universal Power Quality Conditioning System (UPQS), known as universal power quality conditioner, can mitigate the power supply distortion and eliminate the load harmonic current at the same time in power systems. The performance of UPQS or Unified Power Quality Conditioner (UPQC) mainly depends upon how quickly and accurately compensation signals are derived. The steady state and dynamic operation of control circuit in different load current and/or utility voltages conditions is studied through simulation results. The presented method has acceptable dynamic response with a very simple configuration of control circuit. The capacity of series and shunt inverters is calculated through loading calculations of these inverters applying phasor diagram to increase the design accuracy. The results of simulation in MATLAB/SIMULINK software show that the system operates correctly.

Keywords: Active power filter, power quality, unified power quality conditioner, synchronous reference frame theory, inverter loading.

INTRODUCTION

One of the electrical system adapter structures is back to back inverter. According to the controlling structure, back to back inverters might have different operations in compensation. For example, they can operate as shunt and series active filters to simultaneously compensate the load current, harmonics and voltage oscillations. This is called unified Power Quality Conditioner (Akagi and Kanazawa Nabae 1984: Aredes and Watanabe 1995).

The duty of UPQC is decreasing the disturbances which effect the operation of the sensitive loads. UPQC is able to compensate the swell, sag and unbalanced voltage, current and voltage harmonics and reactive power, through shunt and series voltage source inverters. Voltage source inverter has to generate sinusoidal voltage with the frequency, amplitude and the phase determined by the control system. As shown in fig. 1, in order to clear the switching oscillation, a passive filter is applied at the output of each inverter. At the output of shunt inverter, high pass second order LC or first order RC filter is allocated and at the output of series inverter, low pass second order LC or resonance filter is allocated.

UPQC controller provides the compensation voltage through the UPQC series inverter and provides conditioning current through the shunt inverter by instantaneous sampling of load current and source voltage and current. Resulted reference currents are compared with shunt inverter output currents in a hysteresis type PWM current controller.

The required controlling pulses are generated then. Required compensation current is generated by inverter applying these signals to the inverter. Resulted reference voltages are compared with a triangular wave form and required controlling pulses are generated to be applied to series voltage source inverter switches.

In this paper a suitable controlling method has been selected to simulation and the rating of series and shunt inverters has been calculated through loading calculations of these inverters applying phasor diagram to increase the design accuracy.

Selecting the controlling method:

UPQC is vastly studied by several researches as an infinite method for power quality conditioning (Akagi and Fujita 1995: Ming Hu and Heng Chen 2000). Different UPQC controlling methods can be classified in three following classes: time-domain controlling method, frequency-domain controlling method and new techniques. Furrier method is one of the methods can be named as frequency-domain methods. The methods such as P-Q theory, instantaneous reactive power, algorithms based on the synchronous d-q reference frame, instantaneous power balance method, balanced energy method, synchronous detection algorithm, direct detection algorithm and notch filter based controlling method are some can be mentioned for time-domain methods. Dead beat control, space vector modulation and wavelet conversion are some of the new techniques (Mariun *et al*., 2004).

Three general standards considered to select the controlling method are load characteristics, required accuracy and application facility. All methods end in to similar results when the reference signal is calculated

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under balanced and sinusoidal conditions where each ends in to different results under unbalanced and non sinusoidal conditions. Dead beat controlling method presents the best operation among the others but more expense should be paid for its calculations.

Among the introduced methods the reference frame methods seem to be more appropriate. The reason is the fact that it needs sinusoidal and balanced voltage and is not sensitive to voltage distortions and is relatively simple. In result, the response time of the control system shortens. So it's prior to utilize the synchronous reference frame theory in UPQC controlling circuit (Ming Hu and Heng Chen 2000: Mariun *et al*., 2004).

Controller Design:

The control system of proposed system is shown in Fig. 1 which is comprised of three following parts:

a. Shunt inverter control
b. DC link voltage control
c. Series inverter control

Shunt inverter control:

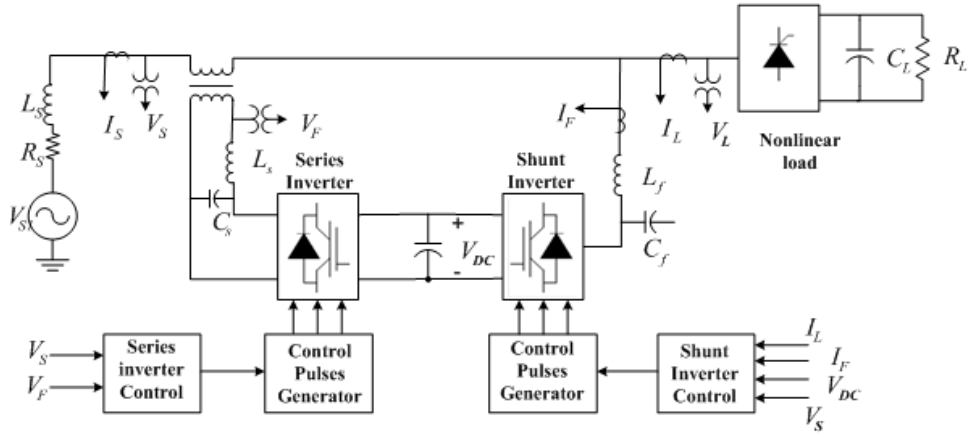


Fig. 1: DC link voltage control block diagram.

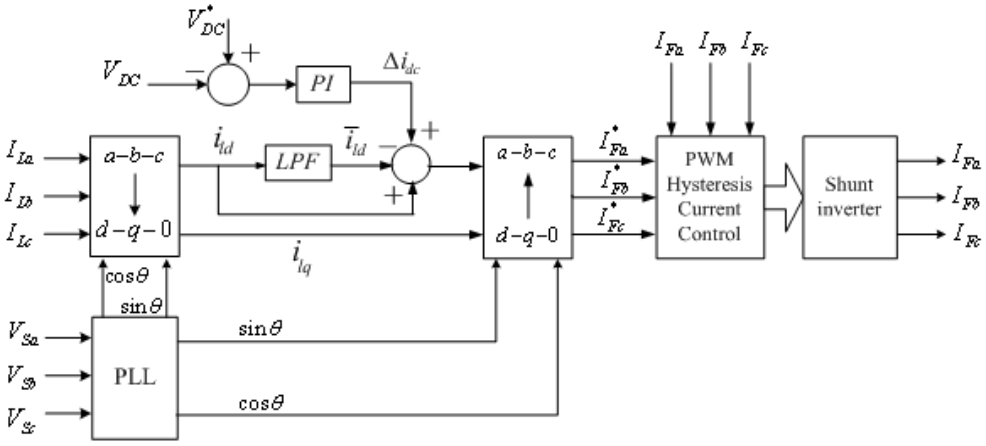


Fig. 2: shows the UPQC shunt inverter controlling block diagram using synchronous reference frame theory(Ming Hu and Heng Chen 2000).

The measured currents of load are transferred into dq0 frame using sinusoidal functions through dq0 synchronous reference frame conversion. The sinusoidal functions are obtained through the grid voltage using PLL. Here, the currents are divided into AC and DC components.

$$i_{ld} = \overline{i}_{ld} + \tilde{i}_{ld} \ , \ i_{lq} = \overline{i}_{lq} + \tilde{i}_{lq} \qquad (1)$$

AC and DC elements can be derived by a low pass filter. Controlling algorithm corrects the system's power factor and compensates the all current harmonic components by generating the reference currents as relation (2):

$$i_{fd}^{*} = \tilde{i}_{ld} \ , \ i_{fq}^{*} = i_{lq} \tag{2}$$

Here, the system currents are:

$$i_{sd} = \overline{i}_{lq} \ , \ i_{sq} = 0 \tag{3}$$

Switching losses and the power received from the DC link capacitors through the series inverter can decrease the average value of DC bus voltage. Other distortions such as unbalance conditions and sudden changes in load current can result in oscillations in DC bus voltage.

In order to track the error between the measured and desired capacitor voltage values, a PI controller is applied. The resulted controlling signal is applied to current control system in shunt voltage source inverter which stabilizes the DC capacitor voltage by receiving required power from the grid. Δi_{dc}, the output of PI controller is added to the q component of reference current and so the reference current would be as relation (4):

$$i_{cd}^{*} = \tilde{i}_{ld} + \Delta i_{dc} \ , \ i_{cq}^{*} = i_{lq} \tag{4}$$

As shown in fig. 4, the reference currents are transferred into abc frame through reverse conversion of synchronous reference frame. Resulted reference currents (i_{fa}^{*} , i_{fb}^{*} and i_{fc}^{*}) are compared with the output currents of shunt inverter (i_{fa} , i_{fb} and i_{fc}) in PWM. Now, the current controller and the required controlling pulses are generated. Required compensation current is generated by inverter applying these signals to shunt inverter's power switch gates.

DC link voltage control:

A PI controller is used to track the error exists between the measured and desired values of capacitor voltage in order to control the D.C link voltage as Fig. 3 (Ghosh and Ledwich 2001).

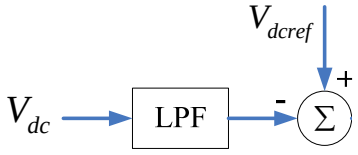


Fig. 3: DC link voltage control block diagram.

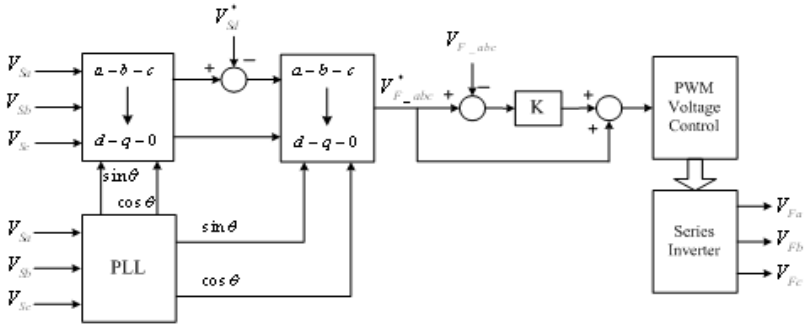


Fig. 4: Series inverter control block diagram.

This signal is applied to current control system in shunt voltage source inverter in a way that the D.C capacitor voltage is stabilized by receiving the required active power from the grid. Correct regulation of proportional controller's parameters plays an important role in D.C voltage control system's response. Too much increase in proportional gain leads to instability in control system and too much reduction decreases the

responding speed of control system. Integral gain of controller corrects the steady state error of the voltage control system.

If this gain value is selected large, the resulted error in steady state is corrected faster and too much increase in its value ends in overshoot in system response.

Series inverter control:

Sinusoidal voltage controlling strategy of load is generally proposed to control the series part of UPQC. Here, the series part of UPQC is controlled in a way that it compensates the whole voltage distortions and maintains load voltage 3-phase balanced sinusoidal. In order to reach this, the synchronous reference frame theory is applied (Ming Hu and Heng Chen 2000).

In this method the desired value of load phase voltage in d-axis and q-axis is compared with the load voltage and the result is considered as the reference signal.

The controlling circuit of series inverter is shown in Fig. 4. SPWM method is used to optimize the response of series inverter.

Series and shunt inverter loading:

Generally, the injected voltage has the same phase with the source voltage when there is balanced voltage source. So, series inverter usually consumes active power. If there is (same phase) injection, UPQC is compensated with the least voltage [10]. Following figures explain the UPQC operation in system's main frequency.

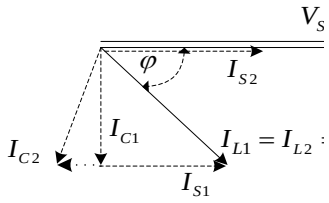


Fig. 5: DC link voltage control block diagram.

The index 1 presents the variable related to the situation faced before the voltage drop occurrence and index 2 presents the situation faced after the voltage drop occurrence. When the voltage and current of the system have the same phases, the transferring power of series inverter is completely active because of the operation of shunt inverter (Basu Das and Dubey 2007). As it is obvious in Fig. 5, shunt inverter current increases by voltage drop occurrence. The reason is the consumption of active power by series inverter through shunt inverter. When the voltage drops in grid, the series inverter should compensate voltage drop to maintain the load voltage 3-phase balanced sinusoidal.

The injected voltage and source voltage are a same phases. This injected voltage and source current also have the same phases. So the series inverter just transfers the active power. As it's obvious in figure, the shunt inverter receives active power from the grid in addition to reactive power injection, as voltage drops. This power is the one that series inverter requires to inject to the grid in order to compensate voltage drop and it is obtained from the shunt inverter through the DC link.

According to the vector diagrams of Fig. 5 following term can be mentioned for each phase:

$$V_{L1} = V_{L2} = V_{S1} = V_o \ \ p.u \tag{5}$$

For load current it can be mentioned that;

$$I_L = I_{L1} = I_{L2} = I_o \ \ p.u \tag{6}$$

Assuming that the UPQC has no losses it can be noted that the electrical power of load side would not change passing the UPQC and will have the same value in the source side.

$$V_S I_S = V_L I_L \cos\varphi \tag{7}$$

As voltage drops V_{S2} is less than V_{S1} ($V_{S2} < V_{S1}$). If *x* is the voltage drop value in pu:

$$V_{S2} = (1-x)V_{S1} = V_o(1-x) \ \ p.u. \tag{8}$$

Following relation should be valid to have the constant active power in both load and source sides:

$$V_L I_L \cos\varphi = V_{S1} I_{S1} = V_{S2} I_{S2} \tag{9}$$

where, I_{S2} can be expressed as follow:

$$I_{S2} = \frac{V_{S1} I_L \cos\varphi}{V_{S1}(1-x)} = \frac{I_o \cos\varphi}{1-x} \ \ p.u. \tag{10}$$

So the nominal power of series inverter ($S_{seinv.}$) is as follow:

$$S_{seinv.} = V_{inj} I_{s2} = \frac{V_o I_o (x\cos\varphi)}{1-x} \ \ p.u. \tag{11}$$

The current injected by shunt inverter in p.u is:

$$I_{C2} = \sqrt{I_{L1}^2 + I_{S2}^2 - 2I_{L1} I_{S2} \cos\varphi} \tag{12}$$

So the nominal power of shunt inverter ($S_{shinv.}$) is:

$$S_{shinv.} = \frac{V_o I_o}{1-x}\sqrt{(1-x)^2 + \cos^2\varphi\{1-2(1-x)\}} \tag{13}$$

Adding the nominal powers of *series* and shunt inverters, the nominal power of UPQC is obtained.

Results shown in Fig. 6 present that the loading of series inverter is similar during low voltage drops for different power factors and is the function of load power factor in high voltage *drops*. If the power factor is high the loading ratio of series inverter is high too. Finally, the maximum loading occurs for unit power factor.

Results shown in Fig. 7 present that in shunt inverter, voltage drop value is the function of power factor and if the power factor is low, the loading is high which seems logical. This is because of the fact that if power factor is low, the shunt inverter should inject more current to compensate the power factor. For high values of voltage drop, the loading of the shunt inverter greatly increases which is because of the fact that series inverter requires more current to compensate the voltage drop. This current is provided by shunt inverter.

Simulation Results:

In this paper, power circuit is modeled as a 3-phase 3-wire system with a non linear load comprised of RC load which is *connected* to grid through 3-phase Diode Bridge. Circuit parameters used in simulation are brought in table (1).

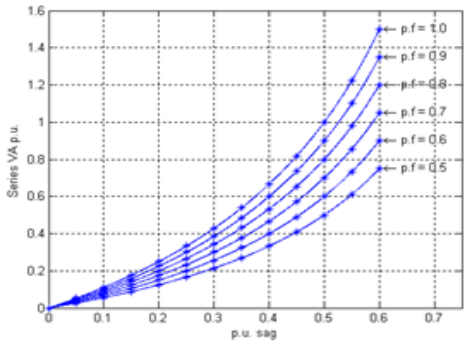


Fig. 6: Comparison of VA loading for series inverter of UPQC at different power factor and p.u voltage sag values

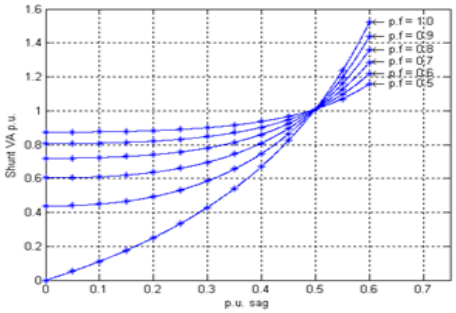


Fig. 7: Comparison of VA loading for series inverter of UPQC at different power factor and p.u voltage sag values

Table 1: Grid Parameters

Parameter	Value
Source Phase Voltage (*rms*)	*220v / 50Hz*
DC Link voltage	*600v*
Shunt inverter rating	*15kVA*
Series inverter rating	*15kVA*
Shunt inverter Inductance (L_f)	*3mH*
Shunt inverter Capacitance (C_f)	*10 μF*
Switching Frequency	*20kHz*
Series inverter Inductance (L_s)	*3mH*
Series inverter Capacitance (C_s)	*15 μF*
Series inverter Resistance (R_s)	*12 Ω*

The simulated load is a RC diode nonlinear 3-phase load which *imposes* a non sinusoidal current to grid with more than 40% THD. Load current is shown in Fig. 8.

In Fig. 9 the source current, injected current and total harmonic *distortion* before and after being compensated by shunt inverter are shown. Shunt inverter is activated in0.04sec of operation. Immediately, the source current is corrected. The results shown in Fig. 9 present that the shunt part has been able to correct the source current appropriately. Also the THD of load current is reduced to 5% from 40% of source current.

Fig. 10 shows the source side voltage, load side voltage and the voltage *injected* by the series inverter to simulate swell and sag of the voltage. As seen in Fig. 10 the voltage distortions imposed to load from the grid are properly compensated by series inverter. In this simulation, series inverter operates at 0.02sec and voltage source faces with 100*v* voltage sag. A voltage swell with 50*v* voltage peak occurs in 0.08sec. Simulation results show that the load voltage is constant during the operation of UPQC series inverter.

D.C link voltage is shown in Fig. 11. In this simulation, series and shunt inverters start to operate at 0.02sec. As it is seen, capacitor voltage is decreasing until this moment. By operating *shunt* inverter, the capacitor voltage increases and reaches to the reference value (600*v*). At 0.04sec of operation voltage sag with 100*v* amplitude occurs in source voltage. The average value of capacitor voltage drops about 10*v* occurring this voltage sag and faces with small oscillations in lower values. At 0.08sec of operation voltage swell with about 50*v* amplitude occurs at 0.08sec of operation. The average value of capacitor increases about 15*v* occurring this swell and faces with small oscillations in voltages around 600*v*.

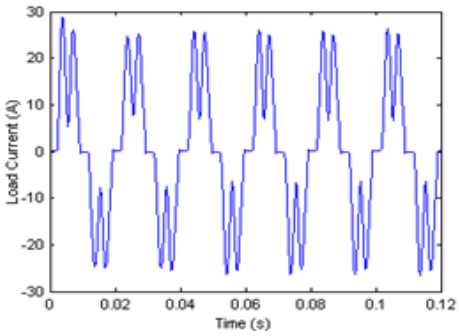


Fig. 8: Nonlinear load current.

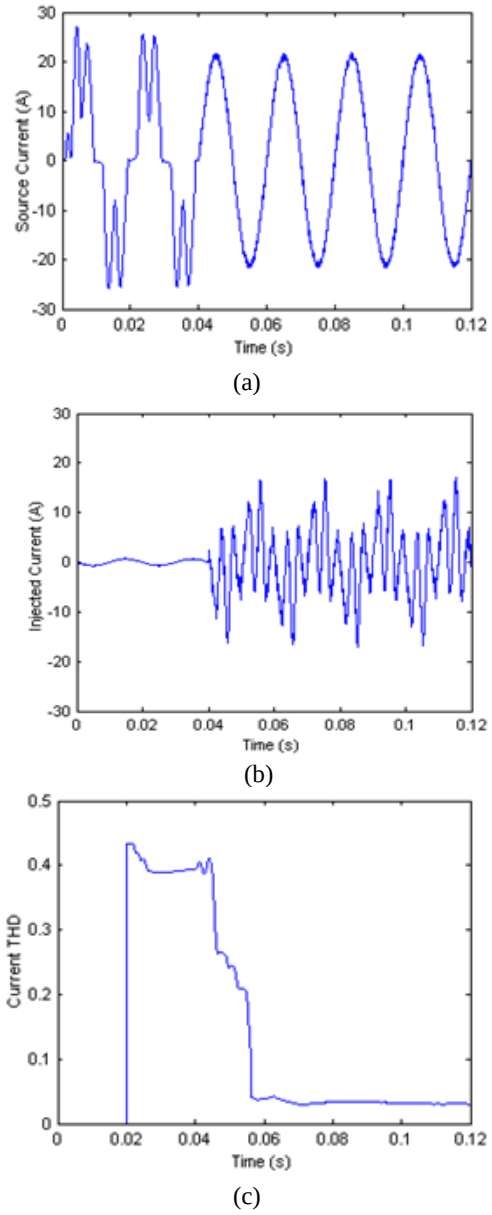


Fig. 9: (a) Source current, (b) Injected current, (c) source current THD, before and after compensation.

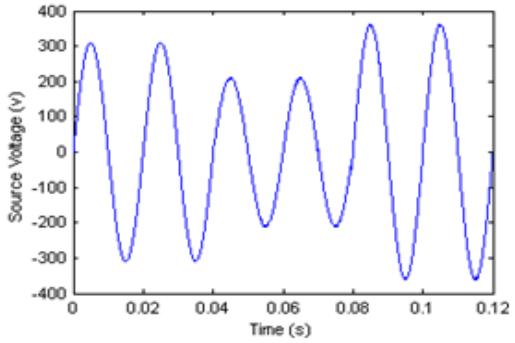
Fig. 11 shows the exact operation of control loop of DC link capacitor voltage. RL load with 6*kW* active power and 6*kVAR* reactive power is applied in simulation to study how reactive power is compensated by shunt inverter. Simulation results show that the phase difference between voltage and current is cleared by shunt inverter operation. In other words, UPQC compensates the reactive power with 0.7 power factor and so there is unit power factor in source side of system. Actually, by operating UPQC, required reactive power is provided via UPQC.

Fig. 12 shows the load current and voltage. As it is shown, load current phase leads voltage phase initially. At 0.06sec of operation and operating shunt inverter the phase difference between voltage and current gets zero.

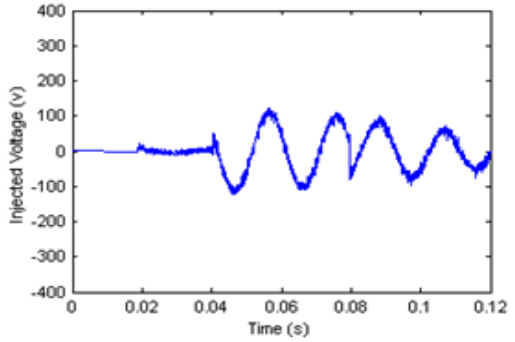
Conclusion:

In this paper unified power quality conditioner (UPQC) is designed and simulated through synchronous reference frame theory. Simulation results show the proposed system's ability in voltage distortion, reactive power and current harmonics compensation. PI controller balances the power between series and shunt inverters by stabilizing D.C link voltage.

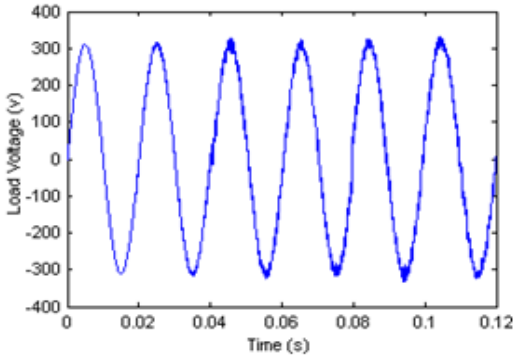
Loading of shunt and series inverters are being operated through phasor method which greatly assists the proper designation of inverters. The operation of proposed system is analyzed using MATLAB/SIMULINK software. Simulation results confirm the correct operation of the proposed system.



(a)



(b)



(c)

Fig. 10: (a) Source current, (b) Injected current, (c) source current THD, before and after compensation.

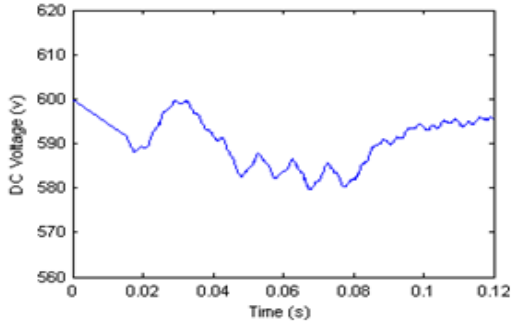


Fig. 11: DC link voltage.

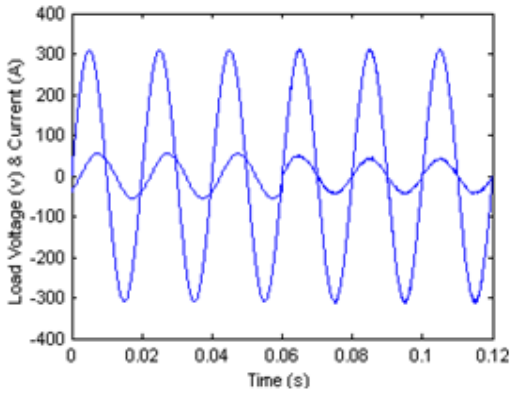


Fig. 12: Power factor correction.

REFERENCES

Akagi, H., H. Fujita, 1995. A new power line conditional for harmonic compensation in power systems, IEEE Trans. Power Del, 10(3): 1570-1575.

Akagi, H., Kanazawa, Y. Nabae, 1984. A., Instantaneous reactive power compensator comprising switching devices without energy storage components, EEE Trans. Industry Application, 20(30): 625-630.

Aredes, M., Watanabe, E.H. 1995. New control algorithms for series and shunt three-phase four-wire active power Filters. IEEE Transactions on Power Delivery, 10: 1649-1656.

Basu, M., S.P. Das, G.K. Dubey, 2007. Comparative evaluation of two models of UPQC for suitable interface to enhance power quality, Electric Power Systems Research, 77: 821-830.

Chen, Y., X. Zha, J. Wang, 2000. Unified power quality conditioner (UPQC): The theory, modeling and application, Proc. Power System Technology Power Con Int. Conf, 3: 1329-1333.

Elkhodary, S.M., M. Khafagy, 2010. Application of Proposed Distribution Network Planning Rules on Fast Developing Countries, Journal of American science, 6(2): 327-335.

Fujita, H. and H. Akagi, 1998. The unified power quality conditioner: The integration of series and shunt-active filters, IEEE Trans. Power Electron, 13(2): 315–322.

Ghosh, A., G. Ledwich, 2001. A unified power quality conditioner (UPQC) for simultaneous voltage and current compensation, Electric Power Systems Research, 59: 55-63.

Mariun, N., A. Alam, S. Mahmod, H. Hizam, 2004. Review of Control Strategies for Power Quality Conditioners, Power and Energy Conference Proceedings, 109-115.

Ming Hu, Heng Chen, 2000. Modeling and Controlling of Unified Power Quality Compensator, IEEE Conf. on Advances in Power System Control, Operation and Management, 2: 431-435.