

A Novel Nanometric Fault Tolerant Reversible Associative Memory Cell

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Abstract: In this paper, two novel fault tolerant reversible SR flip-flop designs are presented. These schemes are used to implement one cell of fault tolerant reversible associative memory. A memory unit accessed by content is called an associative memory or content addressable memory. The main aim is designing novel fault tolerant Reversible match logic for one word of Associative Memory. This circuit with zero internal power is proposed for the first time. The fault tolerant reversible circuit is evaluated in terms of number of reversible gates, number of garbage outputs, hardware complexity and quantum cost. All the scales are in the nanometric area.

Key words: reversible logic gate, fault tolerant, reversible associative memory, reversible match logic.

INTRODUCTION

Information loss is an important challenge which leads to the energy dissipation. The search for energy waste explicitly leads to this question: How much energy per bit is converted to heat? For each irreversible bit operation $KT \ln 2$ joules of energy is required. Where $K = 1.3806505 \times 10^{-23} \text{ m}^2 \text{ kg}^{-2} \text{ K}^{-1}$ (joule/Kelvin) is Boltzmann constant and T is the temperature in degrees Kelvin at which operation is performed (Landauer, 1961). Bennett's researches showed that reversible computing is computing without any information loss (Bennet, 1973). Reversible computing is a model of computing where the computational process to some extent is reversible. In reversible logic the output logical states uniquely define the input logical states of the computational operation. Reversible logic circuits encompass the same number of input and output lines. Such circuits (gates) can produce inputs from the corresponding outputs and vice versa. Reversible logic is a fertile ground for the technological advances. It has many functions in numerous aspects such as optical information process, DNA computing, quantum computing, thermodynamic technology, bioinformatics and nanotechnology. Synthesis of reversible logic circuits are particularly more complicated than the conventional irreversible logic circuits because in reversible logic circuits fan-out and feed-back are forbidden (Haghparsat, 2008; Perkowski, 2001). Recently, researchers illustrated that feedback is allowed in reversible computing in a case of sequential circuits design (Thapliyal, 2010).

In this article, fault tolerant reversible SR flip-flop is employed, to make a very high performance reversible memory cell. Two designs of reversible SR flip-flop are presented. Design #2 is optimized in terms of quantum cost (QC). This work is a preface to design more complex and efficient memory.

MATERIAL AND METHODS

Reversible Circuit:

A reversible circuit is composed of reversible gates that there is a one-to-one relationship between its inputs and outputs. In this section, parity preserving reversible gates such as F2G, NFT, and FRG are briefly described below.

Definition 1:

A reversible gate is a $k \times k$ gate, if it has k inputs and k outputs (Haghparsat, 2008).

Definition 2:

If the output is not used for future computations, the output is said garbage output (Haghparsat, 2008).

Definition 3:

The gate is a parity preserving reversible gate if and only if satisfy the follow equation. For example the equation for a reversible 3×3 gate is: (Haghparsat, 2008).

$$A \oplus B \oplus C = P \oplus Q \oplus R$$

Feynman Gate (FG), is a 2×2 gate that is also called Fan-out gate because it is suitable for single copy of signal which means that if the B input is set to zero then both output lines will result A.

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Fig. 1: (a) Feynman gate, (b) Feynman gate as copying gate.

This gate is named Controlled NOT gate (1- CNOT) it means that if the A input is zero this gate will operate as a buffer gate otherwise it will operate as a not gate. FG is also known as a one through gate because one of the input variables is also repeated in output. Quantum cost of FG is 1 (Haghparsat, 2008).

Feynman Double Gate (F2G), is composed of two Feynman gates hence its QC is 2. This gate is a parity preserving gate therefore it is a fault tolerant gate (Haghparsat, 2008).

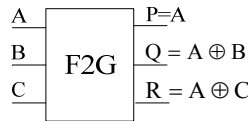


Fig. 2: Feynman double gate.

New Fault Tolerant Gate (NFT), is a parity preserving gate with QC=5. It has three inputs and three outputs. It can implement all Boolean functions. The hardware complexity of this gate is $T_{FRG}=2\alpha+4\beta+2\delta$ which α is a two input XOR gate calculation, β is a two input AND gate calculation and δ is a NOT calculation (Haghparsat, 2008).

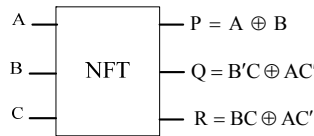


Fig. 3: New Fault Tolerant gate.

Fredkin Gate (FRG), is a swap gate that A input is a control signal which means that if A sets to 1 then the output lines will be swapped else the gate will operate as a buffer. So this gate is called control permutation gate. FRG is a one through gate. FRG is a conservative gate thus it is absolutely a parity preserving gate. The quantum cost of FRG is same as NFT. The hardware complexity of existing gate is as the following equation (Fredkin, 1982).

$$T_{FRG}=2\alpha+4\beta+2\delta$$

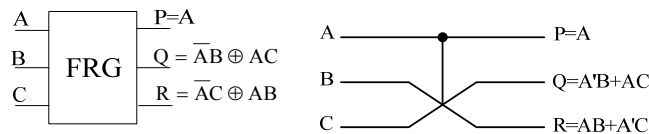


Fig. 4: Fredkin Gate.

Designing of Fault Tolerant Reversible Rising Edge Triggered SR Flip-Flop:

In this article two fault tolerant reversible SR flip-flop designs are presented.

Design #1:

In this approach a fault tolerant reversible SR flip-flop is constructed by means of two fault tolerant reversible SR latches in the form of Master-Slave. In this fault tolerant reversible SR latch fan-out is avoided which is depicted in Fig. 5 (Rice, 2006). As can be seen in Fig. 5 SR latch includes two FRG gates. Fig. 6 illustrates the traditional SR flip-flop circuit. Proposed fault tolerant reversible rising edge triggered SR flip-flop is shown in Figure 7.

According to the Table.1 this circuit is evaluated in terms of number of gates, garbage outputs, quantum cost and hardware complexity.

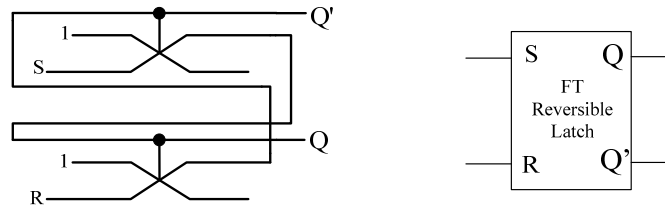


Fig. 5: Fault Tolerant Reversible SR Latch (Rice, 2006).

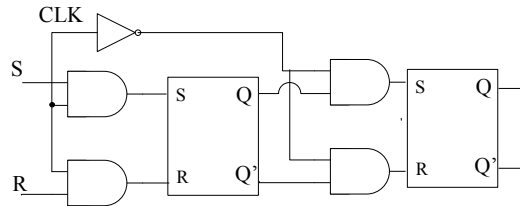


Fig. 6: Traditional irreversible Master-Slave SR flip-flop (Rice, 2006).

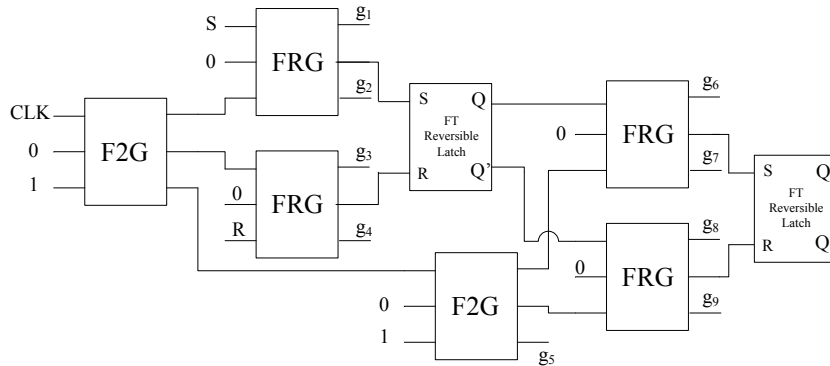


Fig. 7: Proposed fault tolerant reversible rising edge triggered SR flip-flop.

Table 1: Evaluation of proposed circuit in Fig. 7.

	No. of gates	No. of garbage outputs	quantum cost	Total logical calculation
Design #1	10	13	44	$20\alpha+32\beta+16\delta$

Design #2:

In this way, the clock signal is connected to the flip-flop as an input. Traditional edge triggered SR flip-flop's internal circuit is shown in Fig. 8. The edge detector logic circuit that is used in the previous figure is depicted in Fig. 9. Proposed fault tolerant reversible circuits are depicted in Figures 10, 11 respectively.

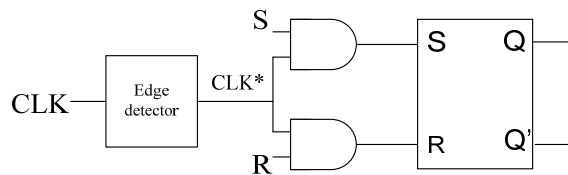


Fig. 8: Conventional irreversible edge triggered SR flip-flop.

The rising or falling edge is generated Because of Not gate's delay in the edge detector logic circuit. As shown in Fig. 11 this delay is generated using two Feynman double gates in proposed reversible circuit.

Number of gates, garbage outputs, quantum cost and hardware complexity are evaluated for this proposed fault tolerant reversible edge triggered SR flip-flop in the Table 2.

Proposed One Cell of Fault Tolerant Reversible Associative Memory:

An associative memory is more expensive than a random access memory because each cell should have the ability to store as well as logic circuits to adapt its content with an external argument (Mano, 2001). Thus, an associative memory is used in applications where the search time is very important and should be short. Block diagram of an associative memory is shown below.

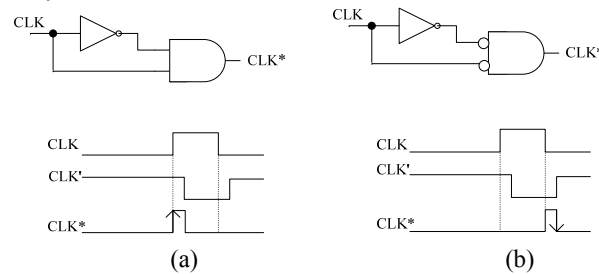


Fig. 9: Traditional irreversible edge detector circuit (a) rising edge, (b) falling edge.

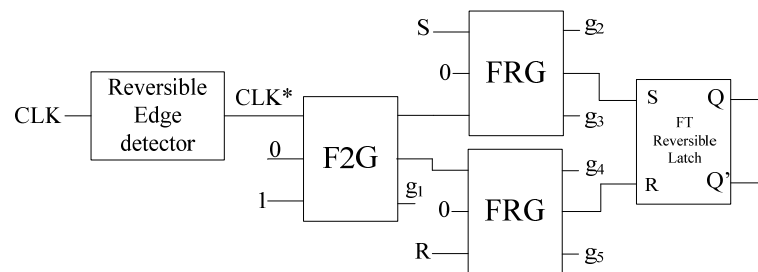


Fig. 10: Proposed fault tolerant reversible edge triggered SR flip-flop.

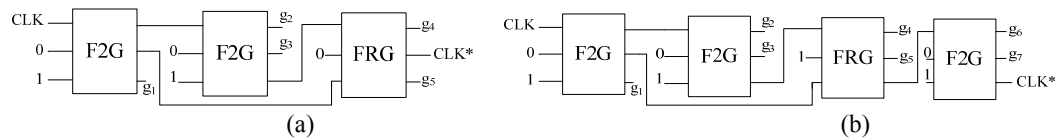


Fig. 11: Proposed fault tolerant reversible edge detector circuit (a) rising edge, (b) falling edge.

Table 2: Evaluation of existing circuit in Fig. 10.

	No. of gates	No. of garbage outputs	quantum cost	Total logical calculation
Design #2 for rising edge	8	12	31	$16\alpha+20\beta+10\delta$
Design #2 for falling edge	9	14	33	$18\alpha+20\beta+10\delta$

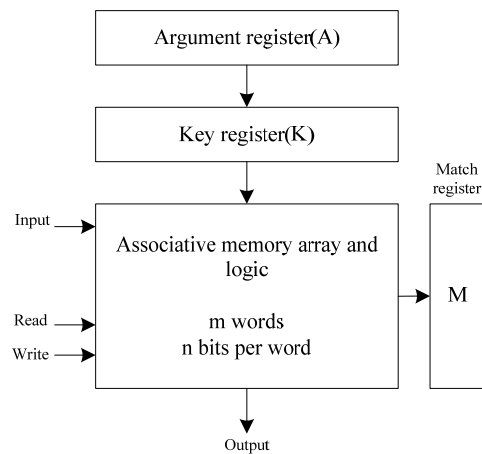


Fig. 12: Block diagram of associative memory (Mano, 2001).

This memory includes m words with n bits. As can be seen associative memory has three registers with the names of argument register A, key register K and match register M. The key register provides a mask for information of argument register in reference to memory. Fault tolerant reversible memory cell is illustrated in Fig.13.

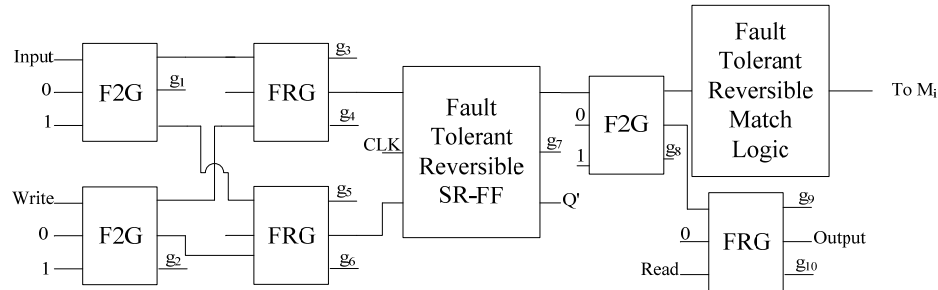


Fig. 13: Proposed one cell of fault tolerant reversible associative memory.

Fault tolerant reversible match logic is designed for comparing the corresponding bit of A_j with the bit stored in the above cell. The words that have compliance with the bits of the argument register, set a corresponding bit in the match register. The following equation demonstrates match circuit operation for every bit.

$$M_i = \prod_{j=1}^n (A_j F_{ij} + \bar{A}_j \bar{F}_{ij} + \bar{K}_j)$$

Proposed fault tolerant reversible match logic for one word of associative memory is depicted in Fig. 14. As can be seen in Fig. 14 one M_i equation is required for each word in the match logic.

RESULTS AND DISCUSSION

Evaluation of The Proposed One Cell of Fault Tolerant Reversible Associative Memory:

As shown in the previous sections, fault tolerant reversible SR flip-flop in design#2 is optimized in terms of number of gates, number of garbage outputs, quantum cost and total logical calculation in comparison with the fault tolerant reversible SR flip-flop in design#1. Evaluation of the presented circuit can be comprehended obviously from the obtained Results.

Table 3: Evaluation of the proposed one cell of fault tolerant reversible associative memory in Fig. 13.

	No. of gates	No. of garbage outputs	quantum cost	Total logical calculation
Scheme1: One cell of memory with SR-ff in Design #1	22	33	89	$44\alpha+60\beta+30\delta$
Scheme2: One cell of memory with SR-ff in Design #2(rising edge)	20	32	76	$40\alpha+48\beta+24\delta$

Table. 3 demonstrates that the proposed parity preserving scheme1 requires 22 gates but the scheme2 with SR flip-flop in design#2 needs 20 gates, so parity preserving associative memory scheme2 is better than scheme1 in terms of number of gates. One of the major parameters in the design of reversible circuits is to minimize the quantum cost. The presented parity preserving scheme2 has $QC=76$. Scheme2 is better than scheme1 in terms of all parameters that is expressed in Table. 3.

4. Conclusion:

In this study, two parity preserving reversible edge triggered SR flip-flop designs are introduced for the first time. Table.1 and Table.2 show the results of two proposed schemes. Proposed fault tolerant reversible edge triggered SR flip-flop can be used in implementation of the parity preserving reversible associative memory cell. In this paper, one cell of fault tolerant reversible associative memory is also presented for the first time. If n fault tolerant reversible associative memory cells are cascaded, then one word of parity preserving reversible associative memory is produced. So this circuit can be applied for m words designing in fault tolerant reversible associative memory. Evaluation of one cell of parity preserving reversible associative memory is observed in Table. 3. All the scales are in the nanometric area.

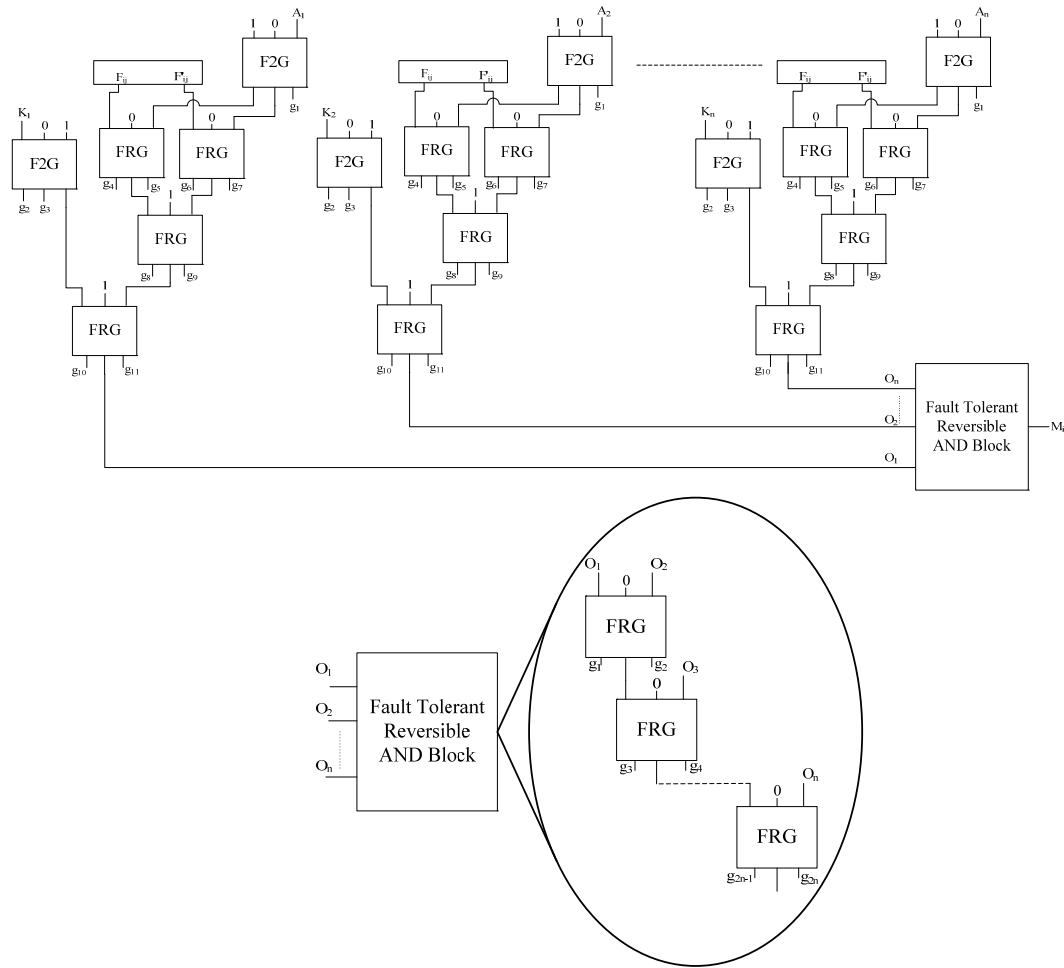


Fig. 14: Proposed Fault tolerant reversible match logic for one word of associative memory.

REFERENCES

- Bennet, C.H., 1973. Logical reversibility of computation. IBM J. Research and Develop., 17: 525-532.
- Fredkin, E. and T. Toffoli, 1982. "Conservative Logic", Int. J. Theor. Phys., 21: 219-253.
- Haghparast, M. and K. Navi, 2008. A Novel Fault Tolerant Reversible Gate For Nanotechnology Based Systems, American J. Appl. Sci., 5(5): 519-523.
- Haghparast, M. and K. Navi, 2008. A Novel Reversible BCD Adder For Nanotechnology Based Systems, American J. Appl. Sci., 5(3): 282-288.
- Rice, J.E., 2006. A New Look at Reversible Memory Elements, in ISCAS.
- Landauer, R., 1961. Irreversibility and Heat Generation in the Computational Process, IBM J. Research and Development, 5: 183-191.
- Mano, M. Morris, 2001. Computer System Architecture, (3rd Edition), Prentice Hall, ISBN: 0130621218.
- Perkowski, M., A. Al-Rabadi, P. Kerntopf, A. Buller, M. Chrzanowska-Jeske, A. Mishchenko, M. Azad Khan, A. Coppola, S. Yanushkevich, V. Shmerko and L. Jozwiak, 2001. A general decomposition for reversible logic. Proc. RM'2001, Starkville, pp: 119-138.
- Thapliyal, H. and N. Ranganathan, 2010. Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay and Garbage Outputs, ACM J. Emerging Technologies in Computing Systems, 6(4).