

4bit,6.5GHz Flash ADC for High Speed Application in 130nm

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Abstract: A 6.5-GS/s 4-bit flash ADC for high speed and ultra wide band application is designed in 130 nanometer CMOS process. Several techniques are used to improve performance of flash ADC. High-speed ADC needs a fast comparator, a high-speed encoder, and a suitable reference ladder. A new comparator used to improve sampling rate of flash ADC. This fully differential comparator consists of three stages using a new structure (domino CMOS logic) to improve its performance. In this paper, used of ballast capacitance to reduce reference voltage deviation at each tap and its effective technique to reduce thermal noise in ladder network. Moreover, the ADC also achieves lower power consumption compared to the earlier design. The flash ADC is able to operate with 2V peak-to-peak input ranges and consume design. The flash ADC is able to operate with 2V peak-to-peak input ranges and consume only 19.83mW. The measured ENOB is 5.42Bits at 6.5GS/s with a 2.2GHz sine wave input signal. The predicted performance is verified by analyses and simulations using HSPICE tool.

Key words: Analog-to-digital converter, Comparator, High speed, Low power, Preamplifier, Decoder.

INTRODUCTION

Flash analog-to-digital converters (ADC) with ultra wide-band (UWB) frequency sampling rates are critical components for applications such as radar, signal capture, satellite, digital oscilloscopes, disk drive read channels, wireless communication, UWB receivers and waveform recorders (Poutlon, 1995). UWB is an emerging technology for short range high data rate communications. The approval of UWB for unlicensed operation in the 3.1-10.6 GHz band under a power emission level of -41.2 dBm/MHz by the Federal Communications Commission (FCC), opened for the public to issue a standard for this communication. Today researchers and the industry have extended the requirement for higher frequency and higher sampling rate. On the other hand, flash ADC has many drawbacks. The first drawback is the hardware complexity. The flash ADC hardware complexity increases exponentially with the resolutions because it needs 2^N-1 comparator circuits. As a result the power dissipation and the chip area also increase exponentially with the resolution. However, the flash ADC is a suitable choice when high speed and low to moderate resolution are required. Flash ADCs published in recent years (Khalilzadeh, 2007; Park, 2006) still have relatively high power consumption and operate with sampling rate lower than the expected future requirement. Hence a new flash ADC structure using an improved comparator is proposed to be used for UWB technology that offer capabilities for the design of communications devices requiring very high performance and low power consumption. In this paper a new CMOS positive feedback and output logic is proposed to increase the speed of track and hold (T/H) of the comparator. The comparator design incorporates various techniques to lower its power consumption and improve its overall performance.

II. Flash ADC Architecture:

Fig.1 illustrates the role of flash ADC in a UWB system. For an "N"-bit converter, the circuit employs 2^N-1 comparators. A 4-bit flash ADC architecture that consists of sample and hold, differential ladder network, comparators and digital back end is proposed. A resistive ladder with 2^N resistors provides the reference voltage. Here two independent resistive ladders are used as a differential reference ladder network. Ballast capacitance is used to reduce the reference voltage deviation, being an effective technique to reduce thermal noise (in high frequency) in the ladder network.

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Fig.2 illustrates the proposed flash ADC block diagram. Figure 2. Block diagram of 4bit flash ADC. The fully differential comparators form a new structure to achieve the overall high speed for the comparators. For the digital design stage MOS Common Mode Logic (MCML) is used with some dynamic logic and buffers. The encoder first converts the thermometer-code into Gray-code, and then generates the respective binary code. Gray-code encoding can also greatly improve metastability. Flash ADCs can generally achieve the higher sampling rates, with the comparator limiting the maximum achievable. Techniques to improve the performance of the ADC are proposed at each of its stages.

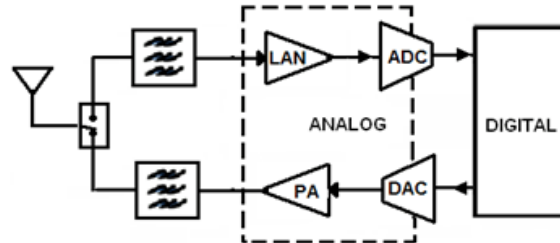


Fig. 1: UWB system.

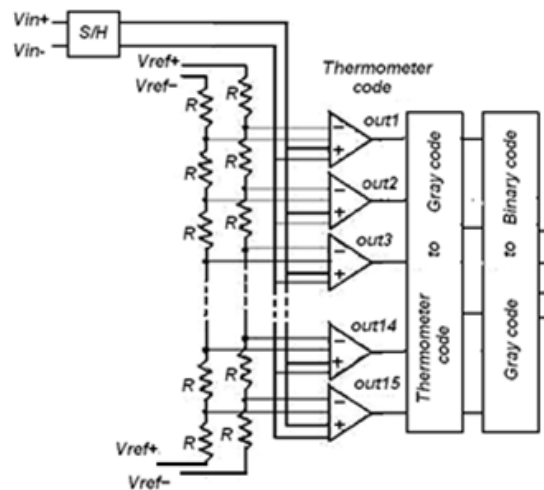


Fig. 2: Block diagram of 4bit flash ADC.

III. Reference Ladder:

There are two design methods for the reference ladder network. Each method has particular advantages and disadvantages. The single structure is preferred when low power consumption and small die area are important, but in the single structure design kickback noise and crosstalk create a big problem for reference voltage at high frequency. In this paper we used two independent resistive ladders as differential reference ladder network, because the flash ADC is used at high frequency. Figure 3. (a) single structure (b) two ladder network.

As shown in Fig.3 the reference voltages are generated by a resistive ladder. This ladder is for 4-bit ADC and has 15 resistors with two redundant resistors on each ladder and generates 16 differential reference voltages for the comparators. All reference voltages for each pre-amplifier, which should be constant under all conditions. The voltage at each tap of the ladder network may change substantially from its nominal DC value and that is a big problem. Therefore, one important source of errors in flash A/D converter is affected by the capacitive feedthrough of the high frequency input signal to the resistive reference ladder. In other words, the signal feedthrough causes variations of the reference voltages.

The middle reference net output V_{mid} is affected the most by the input signal feedthrough. The capacitance feedthrough is simulated by the model of Fig.4 that also shows ladder with capacitance feedthrough effect. Meanwhile, the feedthrough to the midpoint of the ladder as a worst case follows the equation:

$$\frac{V_{\text{mid}}}{V_{\text{in}}} = (4/\pi) \cdot f \cdot R \cdot C \quad (1)$$

After expanding the model to the general case of $2^N - 1$ comparators, R and C are given by:

$$R = R_{\text{tot}} / (2^N - 1) \quad (2)$$

$$C = C_{\text{tot}} / 2^N \quad (3)$$

where R_{tot} is the total reference net resistance, N is number of bits and C_{tot} is the total input. A good estimate of the maximum value of the ladder resistance is given by:

$$R_{\text{Ladder max}} = (V_{\text{mid}} / V_{\text{in}}) / (\pi f_{\text{in}} C_{\text{in.tot}}) = 4\Phi / (2^n \pi f_{\text{in}} C_{\text{in.tot}}) \quad (4)$$

where Φ is the acceptable deviation value of central reference voltage and $C_{\text{in.tot}}$ is total input capacitance and f_{in} is input frequency (Venes, 1996). In addition, resistance is scaled down to achieve a small feedthrough but considerable power-consumption in the reference ladder network (for high input frequencies). Therefore, there is a tradeoff between power consumption and feedthrough. The matching of the different resistors in the ladder network has directly influence on the differential and integral non-linearity of the converter. In this paper is used of ballast capacitance to reduce reference voltage deviation at each tap. This technique play important role to solve charge injection in front of preamplifier, the ballast capacitance is also effective technique to reduce thermal noise (in high frequency) in ladder network.

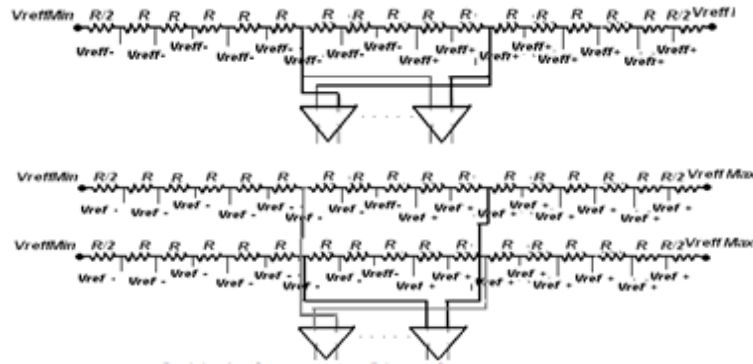


Fig. 3: (a) single structure (b) two ladder network.

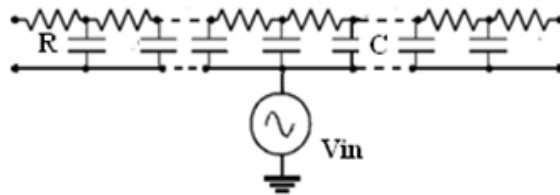


Fig. 4: Model of capacitance feedthrough from input ladder.

IV. Comparator:

A. Comparator Architecture:

The architecture of the comparator is shown in Fig. 5. The comparator structure is fully differential and consists of preamplifier, T/H and output circuits. The first stage is a low gain classical differential amplifier with resistive loads (R_d), which isolates the latches from reference voltages.

The comparator with resistive loads shows better linearity, offset and gain response in comparison with amplifiers with active or diode loads. Low noise amplifier is utilized to reduce the input referred offset of the comparator. The second stage is a CMOS T/H with positive feedback, inductor and current source are used to reduce regenerative time and consists of preamplifier, T/H and output circuits.

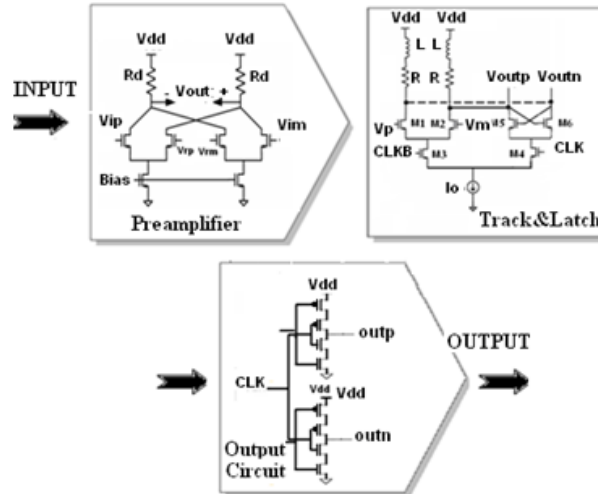


Fig. 5: Schematic of comparator.

There is a question that what aspects of the performance of comparator are important? In addition to power dissipation and speed, such parameters as supply voltage, gain, voltage swings, band width, distortion, input offset, linearity and overdrive recovery may be important. In practice, most of these parameter trade with each other, making the design a multi-dimensional optimization problem. Illustrated in Fig.6 such trade-off present many challenges in the design of high quality comparator for flash ADC, requiring intuition and experience to arrive at an acceptable compromise.

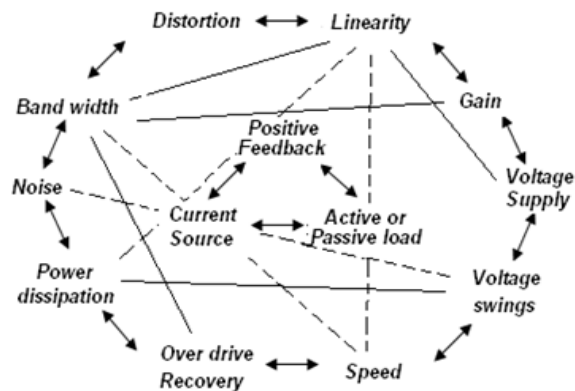


Fig. 6: Relationship between comparator design parameters.

B. Resistive Averaging:

Averaging is a well known method to reduce the input offset of the comparators. Resistive averaging uses some resistors between the outputs of adjacent preamplifiers. This technique has been used in most of the flash ADCs. Fig.7 shows the structure of preamplifier with resistive averaging.

In this method signal-to-noise is improved without extra power consumption. In addition, this is an effective technique to reduce the mismatch impact in comparator arrays. Furthermore, this technique has been used to improve static errors induced due to amplifiers' offset error. The main drawback with this method is that we need over-range comparators to maintain the linearity at the edges.

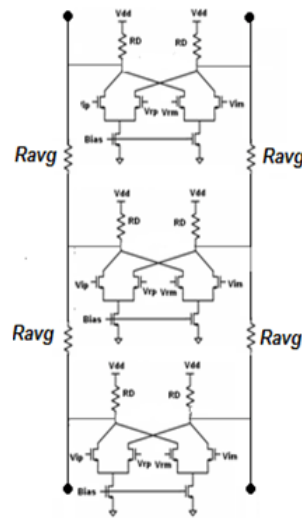


Fig. 7: Resistive averaging in the comparator.

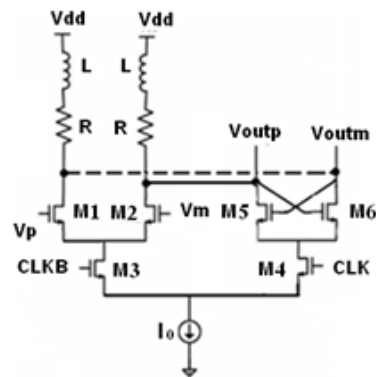


Fig. 8: Comparator core (Track/Hold).

C. Comparator Core (T/H) and Output Circuit:

The comparator core is shown in Fig.8. The load is formed by the series combination of a resistor and an inductor. V_p and V_m are the differential analog inputs signal from the preamplifier. It has input differential pairs (MI and M2) that turn on when the clock is low and track the input from the previous stage. When the clock is high, the comparator goes into hold mode. In this paper CMOS positive feedback is used to improve speed of comparator and reduce the regenerative time in latching mode. The passive inductor peaking technique is also employed in the T/H circuit to enhance the bandwidth (Taghizadeh.,; Mohan, 2000). The domino output circuit as shown in Fig.5 is used instead of SR Latch to support the comparator in high sampling rate operation. The combination of T/H and output circuit (domino CMOS logic) creates a fast structure for the comparator.

V. Encoder Circuit:

The encoder in a flash ADC is very critical and one of the bottlenecks in high-speed operation. Furthermore, the encoder should be able to properly handle comparator metastability and bubble errors in the thermometer code. The schematic of encoder is shown in Fig.9. The encoder is designed using MOS Common Mode Logic (MCML).

This type of design is the most efficient in terms of speed and very low swing signal operation. In other words, MCML circuits allow for operating on low-swing signals of the comparator outputs without converting them full-swing digital signals, therefore its reduced output swing and hence low-power dissipation. The encoder first converts the thermometer-code into gray-code, and then generates the respective binary code. The gray code stage provides only a 1-bit transition between consecutive states and thereby reduces the effects of code skipping and bubble errors at the output of the encoder.

A set of equations (5) shows the conversion from thermometer to gray code and then gray to 4-bit binary code.

$$\begin{aligned}
 G1 &= \overline{C1C3.C5C7.C9C11.C13C15} & B1 &= G1 \oplus B2 \\
 G2 &= \overline{C2C6.C10C14} & B2 &= G2 \oplus B3 \\
 G3 &= C4C12 & B3 &= G3 \oplus B4 \\
 G4 &= C8 & B4 &= G4
 \end{aligned}
 \tag{5}$$

where C is thermometer code, B is bit binary code and G is gray code.

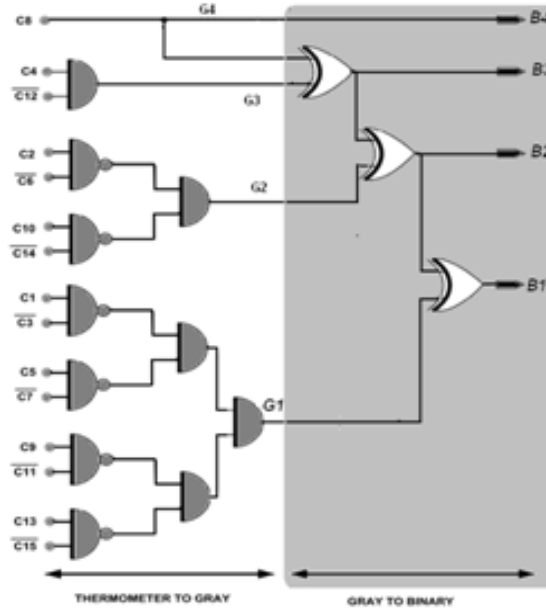


Fig. 9: The schematic of a proposed encoder.

VI. Simulation Results:

The proposed flash ADC structure was designed using 130 nm CMOS technology. Simulation result was obtained by using HSPICE tool. Fig.10 shows the output wave of comparator with 0.5 GHz analog input signal and clock frequency of 6.5 Gs/s. Table I shows the summary of flash ADC, in comparison with the designs in (Khalilzadeh, 2007) and (Park, 2006). Performance Fast Fourier Transform (FFT) is performed to observe the dynamic characteristics of the comparator such as the effective number of bits (ENOB). Fig.11 illustrates FFT of flash ADC at input frequency of 2.2 GHz and sampling rate of 6.5 Gs/s. The new flash ADC dissipates only 19.83 mW at 6.5 GS/s.

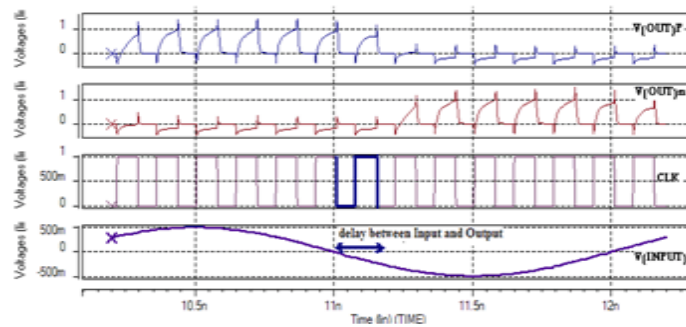


Fig. 10: Output wave of comparator at $F_{in} = 500$ MHz , $F_{clk} = 6.5$ Gs/s.

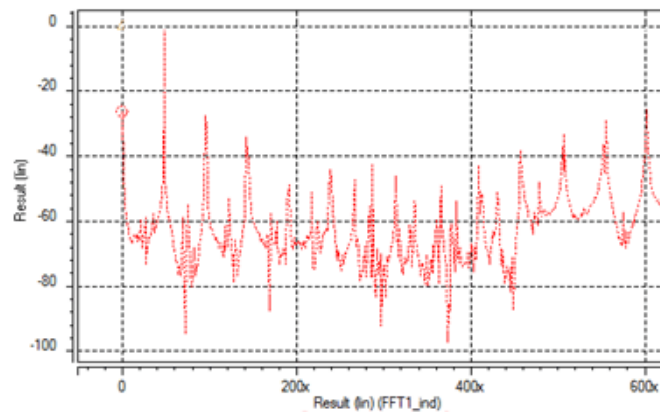


Fig. 11: FFT at input frequency of 2200MHz and sampling rate of 6.5Gs/s

Table I: ADC Performance Comparison.

Item	(Park, 2006)	(Khalilzadeh, 2007)	This work
VDD	1.8 V	1.8 V	2 V
Clock frequency	4 GS/s	4 GS/s	6.5 GS/s
Resolution	4 bit	4bit	4bit
DNL	0.3	0.25 LSB	0.25LSB
INL	0.44	0.35 LSB	0.39 LSB
SFDR	30 dB	-	26.4dB
Power consumption	89 mW	68 mW	19.83 mW
ENOB	3.9	3.4@ $f_{in}=1.5G$	5.42@ $f_{in}=2.2G$
Process	0.18 μm	0.18 μm	0.13 μm
years	2006	2007	2010

Conclusion:

In this paper, a 0.13 μm CMOS flash ADC for high speed, low power and UWB application is proposed. The maximum sampling speed is 6.5 GS/s and the SFDR at 2.2 GHz is 26.4 dB. The analog supply voltage is only 2 V. Several design issues have been discussed and used in the optimization. CMOS positive feedback and a new structure based on domino CMOS logic as output circuit are used to improve sampling rate and performance of comparator. The measured ENOB is 5.42 Bits at 6.5 GS/s with a 2.2 GHz sine wave input signal.

ACKNOWLEDGMENT

The authors would like to acknowledge Dr. Abdolreza Nabavi for his useful suggestion and Microelectronic Laboratory of Tarbiat Modares University, Tehran for software facilities

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