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Design and Analysis of a Two Stage Operational Amplifier for High Gain and High Bandwidth

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Abstract: In this paper a design and comparison between a fully differential RC Miller compensated CMOS op-amp and conventional op-amp is presented. High gain enables the circuit to operate efficiently in a closed loop feedback system, whereas high bandwidth makes it suitable for high speed applications. A novel RC Miller compensation technique is used to optimize the parameters of gain and bandwidth for high speed applications are illustrated in this research work. The design is also able to address any fluctuation in supply or dc input voltages and stabilizes the operation by nullifying. The design is implemented on TSMC 0.18 μm CMOS process at 3.3 V as supply voltage under room temperature 27° C. The simulated result shows that a unity gain bandwidth of 136.8 MHz with a high gain of 92.27 dB is achieved for the proposed op-amp circuit. The total areas of the layouts are 0.000158 mm^2 and 0.000532 mm^2 for conventional and proposed respectively.

Key wrods: Two-Stage Op-amp, fully differential, high gain, high bandwidth

INTRODUCTION

An operational amplifier (op-amp) is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. An op-amp produces an output voltage that is typically hundreds of thousands times larger than the voltage difference between its input terminals (Akter, M., *et al*., 2008; 2008; Reaz, M.B.I., *et al*., 2003; 2005; Reaz, M.B.I., 2007; Marufuzzaman, Mohd., *et al*., 2010) Op-amp circuits are widely used in electronic and communication systems such as differential amplifier, fully differential amplifier, negative feedback amplifier, isolation amplifier, instrumentation amplifier, etc. (Reaz, M.B.I., *et al*., 2006; Reaz, M.B.I. and L.S. Wei, 2004; Mohd-Yasin, F., *et al*., 2004; Mogaki, S., *et al*., 2007). Op-amp, which is first, realized in vacuum tubes manifestos in the 1950s (Amana, Y., 2012). Jin *et al*. brought the first semiconductor engineering with the introduction of integrated circuit (IC) op-amp in 1964 with a low cost, which is widely used in most analog ICs (Jin, F., *et al*., 2011). Op-amp is the key component in analog processing systems. The increasing demand for mixed mode ICs makes the op-amp design to be more critical (Amana, Y., 2012). Op-amp functions as addition or subtraction, integration or differentiation, buffering and amplification. The applications of op-amp are comparators, oscillators, filters, sensors, instrumentation amplifier and many more.

The main challenges of op-amp are to achieve a high dc gain and a high bandwidth with a high output swing depending on the application of use. To achieve a higher gain, multi-stage op-amp can be used by cascading the stages where it can reach until 100 dB of magnitude gain which has been proposed in (Ramirez-Angulo, J., 2007) by using Nested-Miller compensation technique. If the gain stage is increased the bandwidth is reduced, which is the drawbacks of the method. However, it is hard to compensate and stabilize for the two-stage op-amp, which is widely used in many applications (Rosario, M., *et al*., 2003).

Frequency compensation technique is necessary to avoid closed loop instability. Amana proposed the easiest compensation method to connect a capacitor between input and output of the second stage (Amana, Y., 2012). The technique results in pole splitting action and gives high closed loop stability with lower bandwidth. To improve the stability performance, the cascode compensation technique has been introduced (Singh, R. and G. Anu, 2011). The technique improves the settling performance with the limitations of the output swing (Vaibhav, K. and C. Degang, 2009). Single Miller Feed Forward Compensation (SMFFC) technique is proposed by Pugliese *et al*., which alleviates the bandwidth reduction and improves stability (Pugliese, A., *et al*., 2008). However, Gupta disclosed that the previous method suffers from compressed gain bandwidth problem due to the very high gain of the first stage (Gupta, A., 2010). On the other hand, Negative Miller Capacitance Compensation (NMCC) technique, which neglected the undesired capacitances, is also discussed in other research works (Reaz, M.B.I., *et al*., 2007). Thus the bandwidth and the phase margin have been improved.

In this paper, a new RC Miller compensated fully differential two-stage CMOS op-amp is presented. The fully differential topology assists high gain and high bandwidth applications. A current mirror circuit is designed in TSMC 0.18 μm CMOS process without the external biasing voltage sources. High gain makes the circuit to perform efficiently in a closed loop feedback system, whereas larger bandwidth is applicable for high speed

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applications. The design is optimized by choosing the right W/L ratio of the transistors in the circuit. The new design exhibits a higher gain, higher bandwidth and reduces cost in packaging where a single direct current mirror source is utilized.

Conventional Op-Amp:

The traditional or basic op-amp has two differential inputs (positive and negative) and an output. The gain is infinite and the circuit is controllable by the feedback from the output to the negative inverting input (Suk, H.T. and Y. Wong, 2002). Fig. 1 shows a differential op-amp with four feedback resistors.

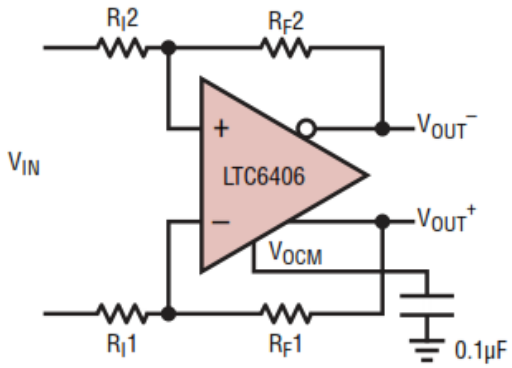

Fig. 1: Differential op-amp circuit with four feedback resistors (Suk, H.T. and Y. Wong, 2002)

The basic circuit of a conventional op-amp is shown in Fig. 2. The circuit consists of a cascade stages where the first stage is the differential amplifier converting the differential input voltage to differential currents. The differential current is loaded by a current sink load, which converts the current to voltage at the output. The second stage is merely the current sink inverter.

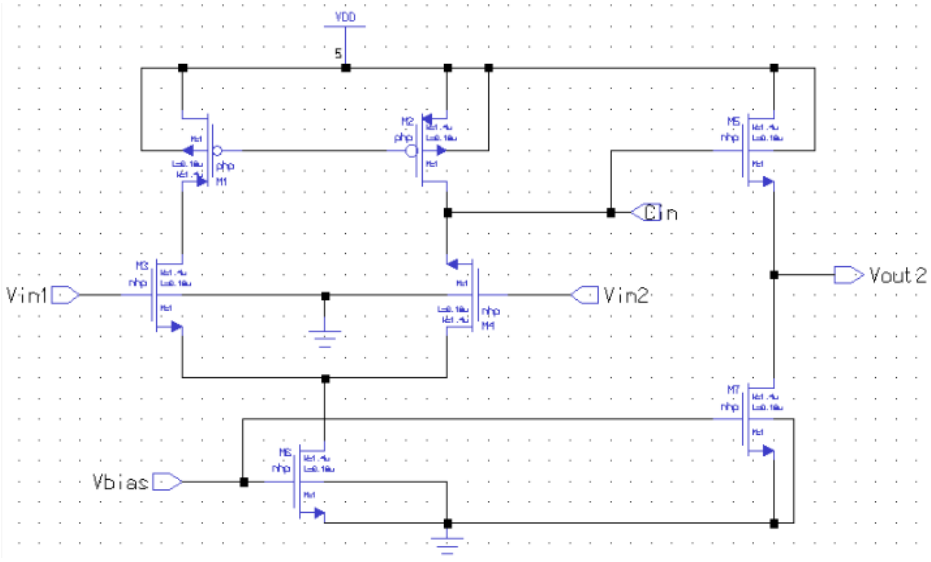

Fig. 2: Schematic diagram of the conventional op-amp circuit

The conventional op-amp is powered by using a high power supply, which causes high power consumption (Parihar, R.K.S. and G. Anu, 2009). Besides that it has stability issue at high gains with high frequencies and may need complementary development for implementation which is costly in terms of production part. Moreover, the conventional op-amp provides inconsistent bandwidth and settling time over a wide range of closed loop voltage gains (Suk, H.T. and Y. Wong, 2002). At low frequencies, generating 180^0 out-of-phase signals is not a critical job, but at high frequencies the effects of non-ideal circuit elements will cause deterioration from the ideal response (Reaz, M.B.I., *et al*., 2007). Conventional op-amp is not applicable for the

down-scaled technology as it is power hungry and causes high cost for fabrication (Suk, H.T. and Y. Wong, 2002).

Proposed Op-Amp Circuit Design:

The proposed op-amp uses RC Miller compensated technique and it is implemented in 0.18 μm CMOS process using libraries from TSMC. Fig. 3 shows the generic 2-stage op-amp with compensation circuit and a biasing circuit. Input amplifier A1 represents the differential pair amplifier and amplifier A2 represents common source amplifier. As for the biasing circuit a single reference current source of 50 μA is utilized where it is free from voltage sources. In the compensation circuit RC Miller frequency compensation is used where a resistor and a compensation capacitor C_c (0.9 pF) is connected in series.

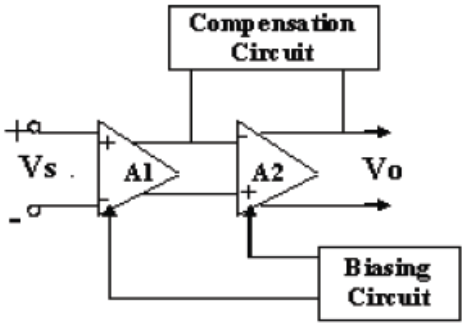

Fig. 3: Two-stage op-amp block diagram (Parihar, R.K.S. and G. Anu, 2009)

By the characteristics of MOS devices it is clear that when a MOS device operates in triode region, behaves like a resistor. In triode region the current through and voltage across the MOSFETs are linearly proportional to each other. To take the advantage of this behaviour, a PMOS device is being used in the design, which consumes very less area in silicon as compared to a resistor. The gate of PMOS has been connected to the ground to ensure that the device will always work in triode region as the source-gate voltage is always high enough than source-drain voltage in magnitude to keep in liner region.

In the proposed design the aspect ratios (W/L) of the transistor is modified to use for the circuit design. Fig. 4 shows the schematic circuit diagram of the proposed op-amp. The circle inside Fig. 5 shows the PMs devices, which acts as the resistor in triode region. Input Iref in Fig. 4 is the single current source used to avoid utilizing voltage sources.

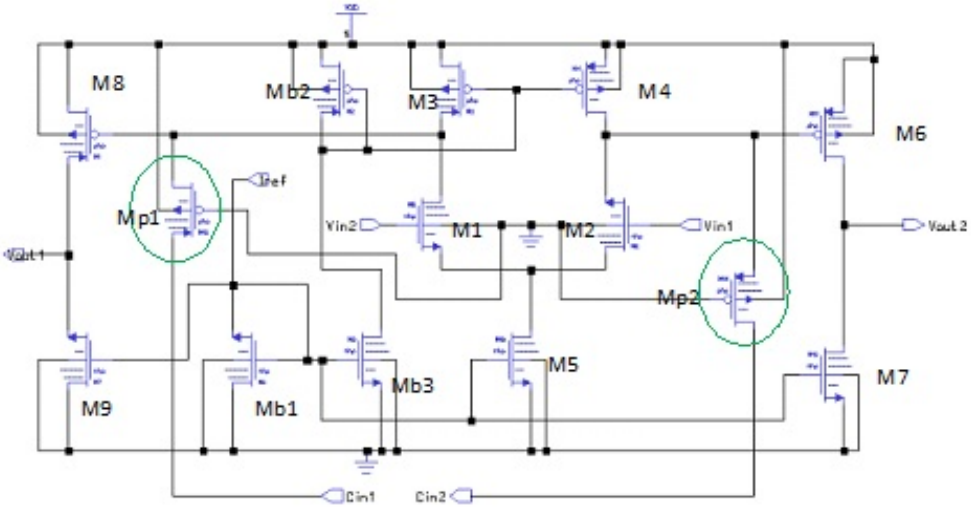

Fig. 4: Schematic Diagram of Proposed Op-amp

To design the proposed op-amp circuit, different sizing of the transistors have been used to achieve the better output results. The aspect ratios of the width and length of the transistors are shown in Table 1.

Table 1: W/L Aspect ratios of the transistors

Transistors	Aspect Ratios (W/L)
M1, M2	12.5/0.18
M3, M4	8.83/0.18
M5	15/0.18
M6, M8	17.7/0.18
M7, M9	7.5/0.18
Mb1, Mb3	2.5/0.18
Mb2	3.06/0.18
Mp1, Mp2	1.825/0.18
Cc1, Cc2	0.9 pF

RESULTS AND DISCUSSION

TSMC 0.18-µm CMOS process is used to measure the output results of the proposed op-amp circuit and the conventional op-amp circuit with the ELDONET simulator. 3.3 V is used as the power supply voltage and 27^{o}C operating condition is used for the simulation of the designed circuits. To set an appropriate operating point, biasing in electronics is the method of establishing predetermined voltages and or currents at various points of a circuit. The operating point of a device, which is known as bias point or quiescent point (or simply Q-point), is the point on the output characteristics to show the DC collector-emitter voltage (V_{ce}) and the collector current (I_c) with no input signal applied. The term is normally used in connection with devices such as transistors.

Fig. 5 shows the simulated waveforms of V_{out} versus V_{in}. The centre point of linear region is marked as Q-point by using the cursor to determine the V_{in}. From the Fig. it is obvious that, V_{in} is obtained 0.632V. The reason for choosing V_{in} within the range is to let the transistors operate under saturation region.

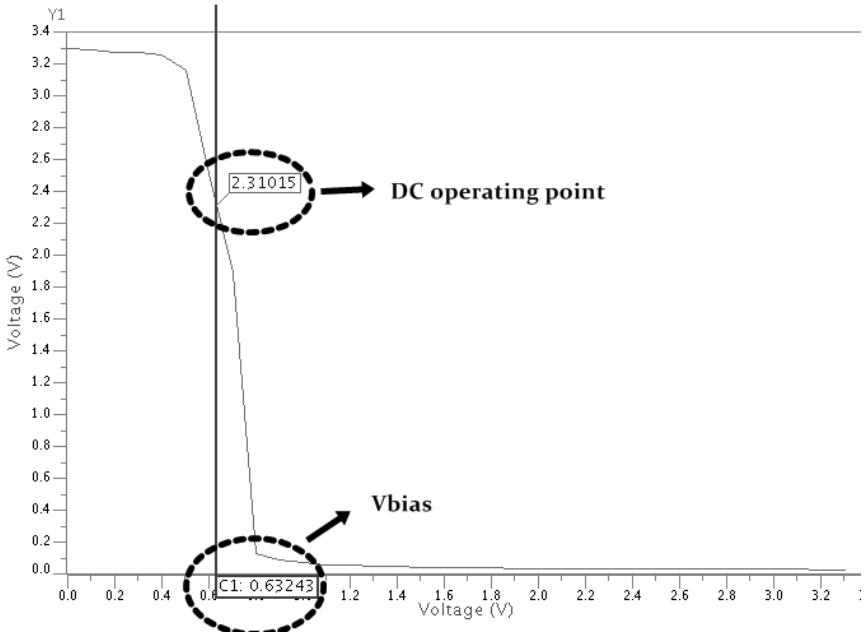

Fig. 5: Simulated waveform of the DC analysis of V_{out} Vs V_{in}, when V_{bias} =0.632V

The analysis is processed only if the V_{bias} fulfilled the requirements. Fig. 5 shows that, V_{bias}= 0.632 V is found for the previous analysis. Substitution of the suitable DC operating bias point produces the value during DC analysis into V_{bias}. The simulated transient analysis of the analysis result of the V_{in} vs time and V_{out} vs time is shown in Fig. 6

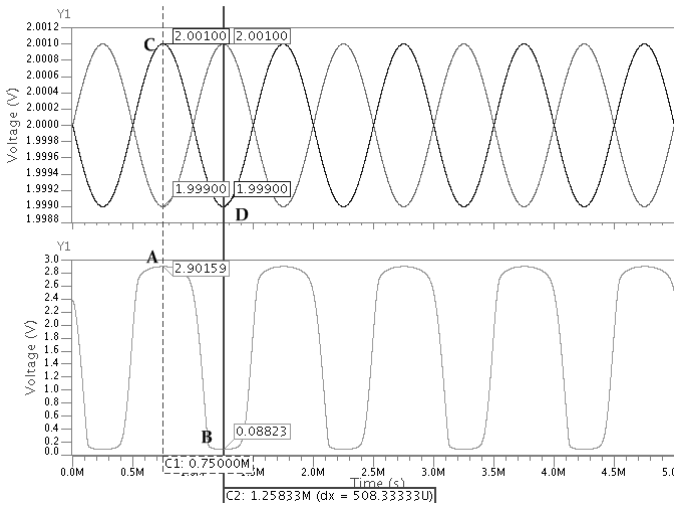

Fig. 6: Transient analysis result of the V_{in} and V_{out}

The simulated waveforms as shown in Fig. 6 prove that the input sinusoidal signal applied is 3.3 mV and -3.3 mV, respectively. To get the gain (Av), and the output sinusoidal signal need to be used to divide with the difference of the input sinusoidal voltage as shown in equation (1). All the values achieved from the simulation results as shown in Fig. 6 are listed in Table 2.

Table 2: Values from Transient analysis of the Fig. 8

V_{in1}-V_{in2}	3mV
V_{out}	2.81336
Gain (Av)	1406.68

$$|A_V| = \frac{V_{out}}{V_{in}} \quad (1)$$

After the successful transient analysis, AC analysis has been done for the proposed op amp circuit. In this case, V_{bias} is remaining the same for second analysis. The frequency from 1 kHz until 10 MHz is utilized for the simulation of the circuits. The simulated output waveform is checked with the gain obtained in previous transient analysis as shown in Fig. 7 to make sure that the desired gain has been achieved for transient analysis for the op amp. Fig. 7 shows the simulated result of the AC analysis. To obtain gain of the op-amp equoation (2) has been utilized.

$$Gain = 20\log_{10}\left[\frac{V_{out}}{V_{in}}\right] \quad (2)$$

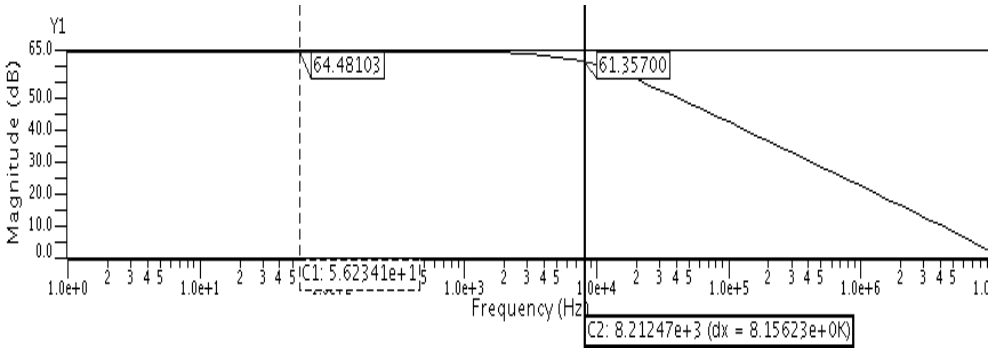

Fig. 7: Simulated results for the AC analysis

Fig. 8 shows the magnitude plot of two-stage op-amp using RC Miller compensation technique. From the result it is clear that a unity gain bandwidth of 136.8 MHz with a high gain of 92.27 dB is achieved. The discrepancies obtained in the post layout simulation are not too far from the ideal one.

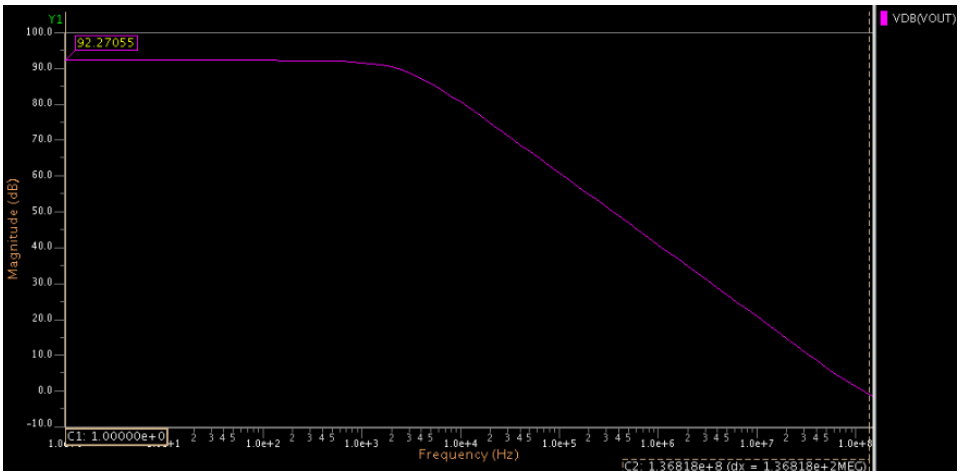

Fig. 8: Magnitude plot of RC Miller compensation op-amp circuit

The pre layout and post layout simulation results shows that the proposed design achieves a higher gain and a larger bandwidth compared to the conventional method. The proposed design saves space in the layout by substituting a PMOS device to the resistor. From the simulation it is proven that when bandwidth increases gain decreases, which is shown in Fig. 9. Moreover, the output is depends on the usage of the applications. If a high bandwidth in GH range is required then a lower gain in the range of 20-30 dB would be obtained.

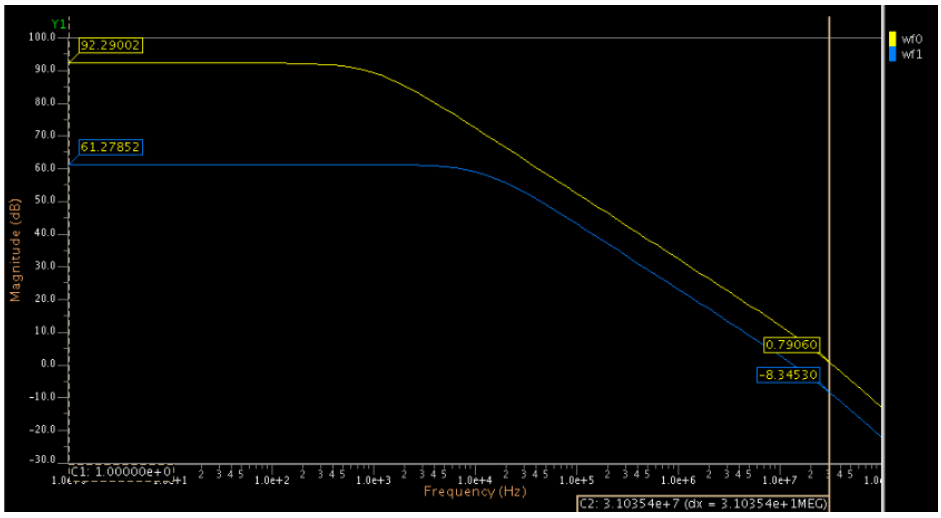

Fig. 9: Simulated results of the Gain and Bandwidth

Designing two-stage op-amps has some advantages and disadvantages to optimize one or more parameters, which may easily result in degradation of others. The main challenge lies on the constant gain bandwidth product, which makes the design parameters more critical. In this research work, the unity gain bandwidth has been improved by increasing the bias current, which leads to reduction in DC gain and increase in power dissipation. However, the design still provides a good alternative to control the increment of the bandwidth. Fabrication of huge resistors in modern VLSI technology could be another problem, which needs to be taken care of. All the limitations are solved by realizing the series resistor for compensation using a PMOS as PMOS always operating in triode region. The design does not use any kind of external voltage source for biasing. Therefore, the packaging cost is reduced by removing additional pins for DC bias voltage sources. A simple looking op-amp design problem becomes a harder one when it comes to optimizing all the parameters at a time. A careful analysis of circuit and deep insight into the circuit topologies and device operations leads to good implementation and desired results.

The complete layout of conventional op-amp circuit is shown in Fig. 10. comparator circuit is shown in Fig. 10. The layout has been compledted using the CEDEC 0.18 um CMOS process. The layout area of the conventional op-amp circuit is found 15.18 x 10 um with the MOSFETs.

Conclusion:

In this paper, a new RC Miller compensation technique is used to optimize the parameters of gain and bandwidth for high speed applications. In VLSI design, power consumption and area are the two major things for applicable devices. Moreover, comparison study shows that, the proposed op-amp circuit produced better performance in terms of gain bandwidth than the conventional op-amp circuit. The simulation outputs are found satisfactory using TSMC 0.18 µm CMOS process. Moreover, by removing additional pins for DC bias voltage sources the packaging cost is reduced. In addition, all the limitations of the conventional design are solved with the realizing of using all the resistors in series resistor to compensate of using PMOS transistors.

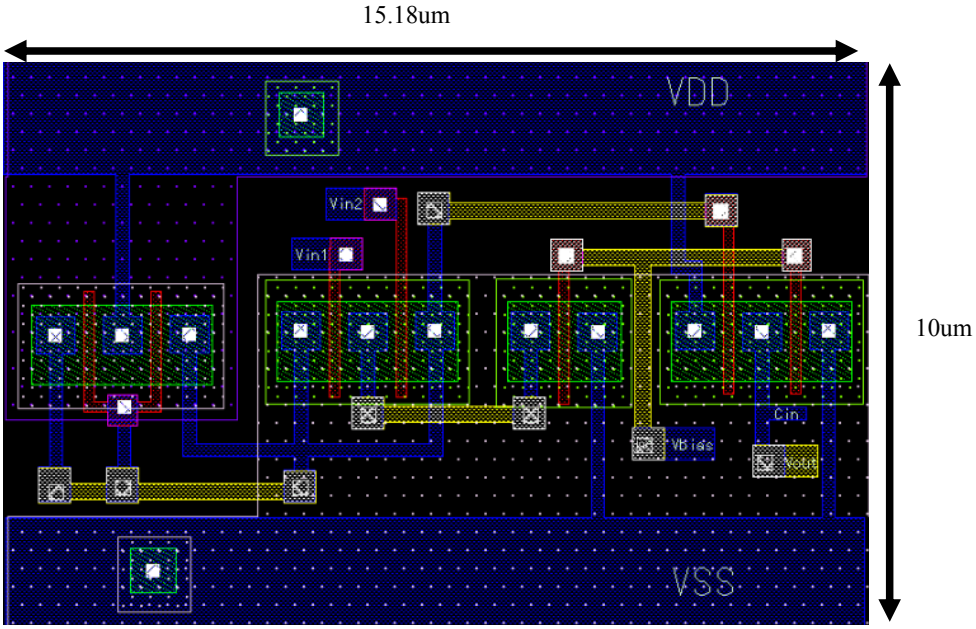

Fig. 10: Layout diagram of the conventional Op-amp circuit

On the otherhand, the layout for the proposed op-amp circuit is shown in Fig. 11. In this case, the layout area for the designed proposed op-amp circuit is incresead with the large number of transistors. The size of the layour is found 29.08 x 18.32 um. From the layout as shown in Fig. 11, the circuit is using standard METALs (MET1 and MET2) for the internal connectivity of the circuitry.

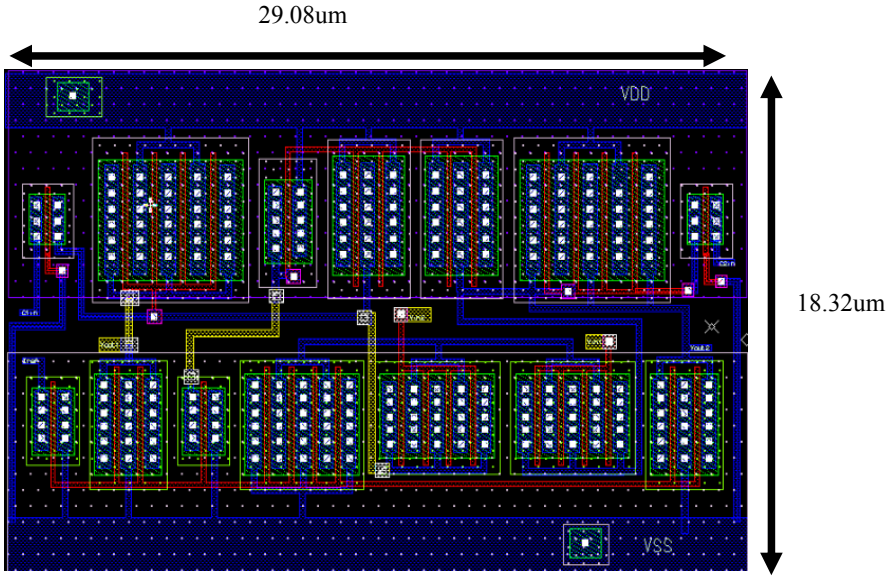

Fig. 11: Layout diagram of the proposed op-amp circuit

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