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Quantum Analysis of Transconductance-Gate Source Voltage Characteristic of Gate-All-Around CdSe Nanowire Field-Effect Transistor

Seyed Ali Sedigh-Ziabari

Department of Electrical Engineering Roudbar Branch, Islamic Azad University, Roudbar, Iran

Abstract: we simulate the gate-all-around CdSe nanowire field-effect transistor (GAA CdSe NWFET) with nonequilibrium Green's function (NEGF) method. We have divided the I_{DS}-V_{GS} characteristic into three regions of operations in terms of V_{GS}. Region 1 includes $0 \le V_{GS} \le |E_{FS}/q|$=0.16 V, region 2 covers the voltage range of $|E_{FS}/q| \le V_{GS} \le |(E_{FD})/q|$=0.56 V, and region 3 includes $V_{GS} \ge |(E_{FD})/q|$. We have shown that there exists a region of gate-source bias over which of the device transconductance experiences a negative slope. Finally, we have analysed transconductance-gate source voltage characteristic treatment.

Key words: CdSe Nanowire field effect transistor (NW-FET); transconductance; channel transmission probability.

INTRODUCTION

The gate-all-around nanowire field-effect transistors (GAA NWFETs) are a promising option for nanometer transistors and recently they are being studied widely (Wang, J., 2005; Mincheol Shin, 2007; Sedigh-Zyiabari, S.A., 2011; Abul Khayer, M., 2008; Abul Khayer, M., Roger K. Lake, 2009). Extensive research has been carried out on the GAA NWFETs made of the semiconductors group IV such as silicon (Wang, J., 2005; Mincheol Shin, 2007; Sedigh-Zyiabari, S.A., 2011), group III-V such as InAs and InSb (Abul Khayer, M., 2008; Abul Khayer, M., Roger K. Lake, 2009), and group II-VI such as ZnO (Steve J. Pearton, 2008). CdSe is another option to construct GAA NWFETs (Khandelwal, A., B. Tech, 2005; Khandelwal, A., 2006). The electron effective mass in the CdSe is less than that in Si, and its nanowire can be covered with SiO_2 (Khandelwal, A., B. Tech, 2005; Khandelwal, A., 2006). In this paper, we specifically investigate the bias dependence of the drain source current in a GAA CdSe NWFET.

The remaining part of this paper is organized as follows. In Section 2, a brief overview of the device structure is introduced. Section 3 is dedicated to the simulation results and discussion. Finally, the conclusions are drawn in Section 4.

2. Device Structure:

A schematic representation of a gate-all-around CdSe nanowire field-effect transistor (GAA CdSe NWFET) is shown in Fig. 1. The oxide layer is assumed to be SiO_2 with a thickness of d_{ox}=5 nm. The corresponding source Fermi levels would be E_{FS}=−0.16 eV, at thermal equilibrium. In this transistor, the channel diameter and length are taken to be d_{ch}=5 nm and L_{ch}=10 nm, respectively.

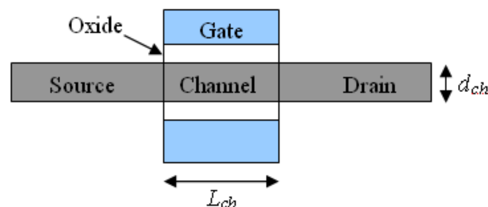

Fig. 1: Cross section side view GAA CdSe NWET.

RESULTS AND DISCUSSION

This device is simulated by the nonequilibrium Green's function (NEGF) method assuming electron's ballistic transport (Abul Khayer, M., 2009; Datta, S., 2005). Figure 2 shows the drain-source current (I_{DS}) versus the gate-source voltage (V_{GS}) of the transistor shown of Fig. 1 with L_{ch}=10 nm, for V_{DS}=0.4V. As depicted in this figure, we may divide the I_{DS}-V_{GS} characteristic into three regions of operations in terms of V_{GS}. Region 1 includes $0 \le V_{GS} \le |E_{FS}/q|$=0.16 V, region 2 covers the voltage range of $|E_{FS}/q| \le V_{GS} \le |(E_{FD})/q|$=0.56 V, and region 3

Corresponding Author: Seyed Ali Sedigh-Ziabari, Department of Electrical Engineering Roudbar Branch, Islamic Azad University, Roudbar, Iran.
E-mail: sedigh@iauroudbar.ac.ir

includes $V_{GS}\geq|(E_{FD})/q|$. Notice $E_{FD}=E_{FS}-qV_{DS}$. To explain the device behavior in each of these three regions, we plot the channel transmission probability $T(E)$ spectra, as illustrated in Fig. 3. Note that the channel current is proportional to $\int dET(E)[f_S(E-E_{FS})-f_D(E-E_{FD})]$, wherein $f_{S,D}$ represent the source and drain occupation probabilities. Figure 3 shows three plots of $T(E)$ obtained for V_{GS}=0.1 V (solid line) that falls in Region 1, V_{GS}=0.3 V (dashes) that falls in Region 2, and V_{GS}=0.6 V (dot-dash) that falls in Region 3, all three are obtained for V_{DS}=0.4 V. The two blocks on the left and right represent the source with Fermi level of E_{FS}=−0.16 eV and the drain with Fermi level of E_{FD}=−0.56 eV. From the solid line in Fig. 3, one can realize that the contribution of $T(E)$ in the current in region 1 is limited to the electrons coming from the source with energies higher than the source Fermi level (i.e., $E\geq E_{FS}$). On the other hand, the number of electrons in this region is negligible since $f_S(E-E_{FS})|_{E>E_{FS}}\sim 0$. Hence the transistor is in the OFF state when operating in region 1. In region 2, contribution from $T(E)$ to the device current, as can be realized from the plot shown by the dashes in Fig. 3, mostly comes from electrons with energies $E_{FD}\leq E\leq E_{FS}$. In such condition, obviously, $f_S\sim 1$ and $f_D\sim 0$. Hence, the current for any given V_{GS}, in this region, can be approximated by the area under the $T(E)$ curve for that particular V_{GS}. That is, $I_{DS}(V_{GS})\propto \int dET(E)|_{V_{GS}}\equiv\Theta(V_{GS})$. In region 3, where $V_{GS}>|E_{FD}/q|$, the rate of increases in I_D decreases until $V_{GS}\rightarrow|(E_{FD}-\text{a few } kT)/q|$, after which the current saturates.

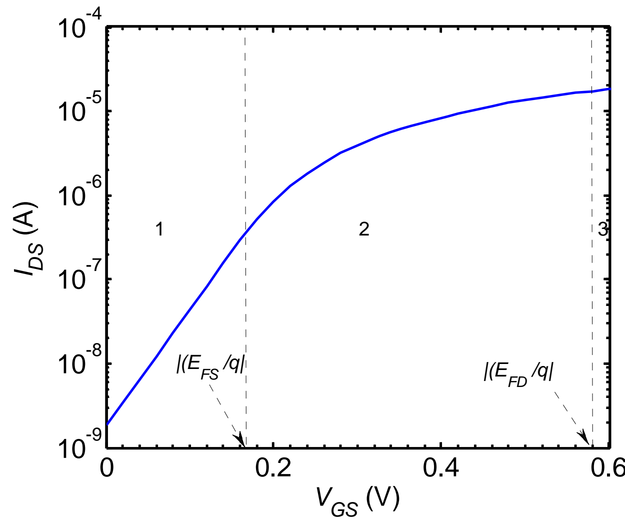

Fig. 2: I_{DS}-V_{GS} characteristic for the GAA CdSe NWFET.

By differentiating the current with respect to V_{GS}, we can obtain the channel transconductance (i.e., $g_m=\partial I_D/\partial V_{GS}$). Figure 4 illustrates the plot of g_m versus V_{GS}, obtained from the data shown in Fig. 2. As seen in this figure, there are two biasing ranges (in region 2) over which the transconductance experiences negative slope which is a non-classical phenomenon. The first rang is over 0.28 V<V_{GS}<0.34 V and the second range V_{GS}>0.46 V. This phenomenon can be explained by taking a careful look at the variations in the area under the transmission curves as V_{GS} increases incrementally. Now, by increasing V_{GS} by increments of ΔV_{GS}=10 mV, we calculate the relative $\Delta\Theta/\Theta=(\Theta(V_{GS}+\Delta V_{GS})-\Theta(V_{GS}))/\Theta(V_{GS})$ and plot the resulting data as illustrated in Fig. 5.

Comparison between Figs 4 and 5 shows that reveal that both curves follow a similar behavior. That is, the curve for $\Delta\Theta/\Theta$ in Fig. 5 experiences a peak at V_{GS}=0.28 V then falls to a minimum at V_{GS}=0.34 after which increase until reaches maximum value at V_{GS}=0.46, and then experiences a negative slope again. Comparison of Fig. 4 with Fig. 5, reveals the reason behind the negative slopes in g_m-V_{GS} plot.

4. Conclusion:

In this paper, we have simulated the various characteristics of the gate-all-around CdSe nanowire FETs, such as their I_D-V_{GS}, transconductance, g_m, using NEGF method. We have divided the I_{DS}-V_{GS} characteristic into three regions of operations in terms of V_{GS}. Region 1 includes $0\leq V_{GS}\leq|E_{FS}/q|$=0.16 V, region 2 covers the voltage range of $|E_{FS}/q|\leq V_{GS}\leq|(E_{FD})/q|$=0.56 V, and region 3 includes $V_{GS}\geq|(E_{FD})/q|$. We have discussed about the quantum mechanical phenomenon that causes the slope of g_m-V_{GS} to be negative over a specific range of V_{GS}.

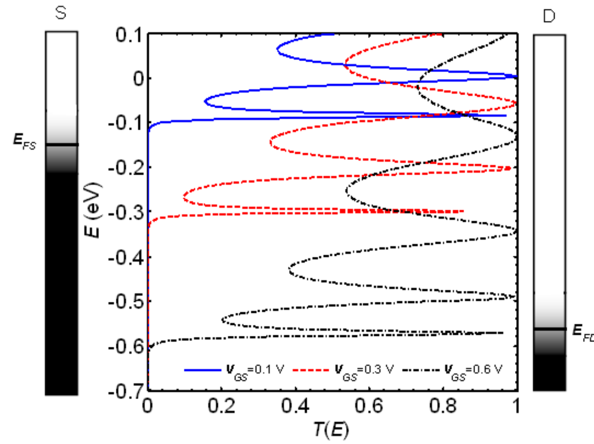

Fig. 3: Transmission probability spectra for electrons across the channel of length L_{ch}=10 nm, for V_{GS}= 0.1 V, V_{GS}=0.3 V, and V_{GS}=0.6 V.

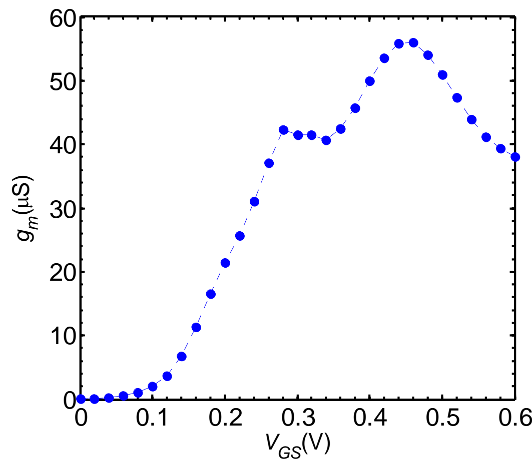

Fig. 4: Plot of g_m versus V_{GS}, for the transistor with L_{ch}=10 nm and V_{DS}=0.4 V.

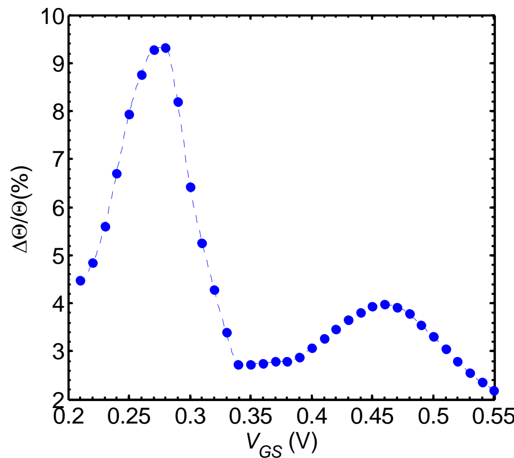

Fig. 5: Variations in the area under the transmission curves as a function of V_{GS}, for the transistor with L_{ch}=10 nm and V_{DS}=0.4 V.

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