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Advanced Cmos Based Image Sensors

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Abstract: Complementary Metal Oxide Semiconductor (CMOS) Image Sensors technology since their innovation has been changed a lot. Previously, CMOS technology was not so powerful to be considered as the competitor with couple charged devices. However, current CMOS Image Sensors (CIS) gain a huge market share by offering many advantages such as lower voltage operation, on-chip functionality and low cost. Nevertheless, they have the noise and low sensitivity problems. There are variousCIS to satisfy the huge demand in different areas, such as digital photography, industrial vision, medical and space applications, electrostatic sensing, automotive, instrumentation and 3D vision systems. Recently, a lot of research is done to solve the problems of sensitivity, noise, power consumption, voltage operation, speed imaging and dynamic range. In this paper, advanced CIS are reviewed, gathering data on the newest advances, their applications and the recent challenges.

Key words:

INTRODUCTION

Visual information is the most intuitive information perceived by human. Image sensors are able to provide the visual information for recognition, monitoring and surveillance. Due to the of low power consumption CMOS, system integration has become much easier (Reaz and Wei 2004; Mohd-Yasin *et al*. 2004; Reaz et. al. 2006; Mogaki *et al*. 2007; Akter *et al*. 2008a, b; Reaz *et al*. 2007a, b; Marufuzzaman *et al*. 2010; Reaz *et al*. 2003; Reaz *et al*. 2005). CIShas become a viable alternatives to charge coupled devices. CIS are used for capturing images digitally. In a CMOS sensor, each pixel has its own charge-to-voltage conversion, and the sensor often also includes amplifiers, noise-correction, and digitization circuits. In 1969, Boyle and Smith improved the charge coupled device. That was the revolution of the digital images. However, that technology had lot of problems as that was the first generation of digital components. In 1995, in the laboratory of NASA, researchers made CIS for space devices that had more advantages over the older methodsspecially in power saving. Research of Fossum led to the improvement of active-pixel sensors that consisted of many on-chip operations, used in portable devices, lower power operation, and high resolutions systems (Isaak *et al*. 2010).

During 1995 till 2001, the first company which developed the CIS was Photobit. This company designed successfully the first high-speed machine vision solutions used for dental radiography. In 2001, a major manufacturer for semiconductor memory was Micron Technology which innovated a new branch of business with the usage of CMOS image sensors.The combination of Photobit and Micron's technology was a kind of magic. Commonly, Dynamic Random-Access Memory (DRAM) process and CMOS image sensor process was near to each other. In addition, Micron's Imaging Group understood that there was another benefit for DRAM. In DRAM memory cells, which are very similar to pixels, need to hold a charge. So, memory processes produce should be very low noise cells and therefore best-quality imagers.

Lots of imagers during that time were using logic semiconductor processes. Thesewere normally designed to transfer charges very quickly with low noise they produced. Therefore, CMOS image quality increased with sharpness and clarity.After Micron Imaging, in2006, Avago Technologies' included the greatest engineering in imaging and the CMOS advanced very quickly. During recent years, the first user of CIS is Micron's Imaging group. Also Micron CMOS sensors are used into one of every three camera phones on Earth in the last years.

CIS has widely been used due to their advantages of low voltage, low power, and on-chip integration capability compared with chargecoupled device sensors. Recently, ultralow-voltage and low-power CIS have been required for new applications such as wireless sensor networks and biomedical systems.The image sensor is compulsory for personal camera and some security camera and cell phones and in order to have the best picture for recognition. Three category is sorted for cameras, in which the first one is personal cameras that have the best marketing because the usage of CMOS sensors and some features in it.

Readout Method And Analog To Digital Converter Development:

CMOS has particular fabrication technology to optimize the photography and charge transferring data. One of the advantages of this special technology is to minimize the pixels size. Although, the other function of

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camera cannot be added in the same chip and more chips for couple charge devices technology is required. For reading the data on the column in couple charge devices, shift style read out method is used to read the datadirectly from each pixel (Gamal and Eltoukhy, 2005). Figure1 shows the difference between reading data of CMOS and couple charge device.

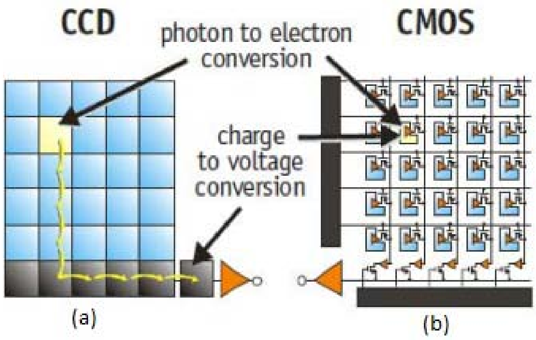

Fig. 1: (a) reading data on couple charge devices (b) reading data on CMOS (Lustica, 2011)

Due to the benefit of low power consumption and easy system integration with on-chip circuits, recent advances in CIS have made them viable alternatives to chargecoupled devices, particularly in high-speed videographer. There exist three architectures for Analog to Digital Converter (ADC) integration in CIS, a single-channel ADC, a pixel-level ADC, and a column-parallel ADC. The single-channel ADC uses a single ADC for an entire pixel array. Hence, extremely high-speed ADC should be required to achieve a high frame rate. The pixel-level ADC implements an ADC in every pixel, providing extremely high frame rate at the price of silicon area and power consumption. The column-parallel ADC which has an ADC in each column can achieve a good tradeoff among frame rate; fill factor, silicon area, and power consumption. Therefore, the column-parallel architecture is the most widely used architecture for both low-speed mobile imager and high speed high-performance imager.

Cis Circuits:

CIS are mainly of four types. They arePassive Pixel Sensor (PPS), Active Pixel Sensor (APS), Pinned Photodiode (PPD) and Digital Pixel Sensor (DPS). These types are discussed below.

PassivePixel Sensor (PPS):

PPS was the first generation of CIS, where an inner pixel (transistor) is selected for charge collection which flows out to the column read out. This data is in current mode and changed by a particular amplifier to the voltage at the end of the column. Whilst, a small current into the big capacitor causes exigent noise and this is one of the biggest problems in passive pixel. The quality of PPS was less than couple charge devices strategy.Thus, at first CMOS did not have any superiority overcouple charge devices. The only merit of PPS is the reduced of pixel dimensions (Lustica, 2011).Figure 2 shows the PPS.

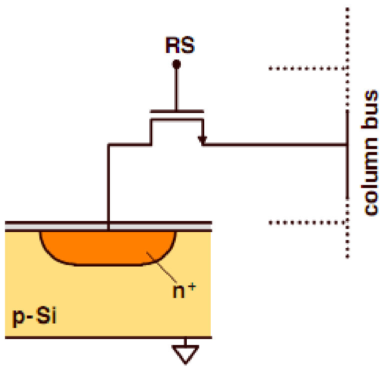

Fig. 3: Diagram of passive pixel sensor (PPS) (Theuwissen, 2011)

Active Pixel Sensor (APS):

The situation of amplifier has been changed and located in the pixels which amplified the charge of the pixel and send it to analog signal processor. With this method, the noise will be decreased.APS has solved the problem of PPS while the cost of this kind of sensors is increased due to the increment of transistors. There are two kinds of APS: three transistor APS (3-T) and four transistor APS (4-T). In 3-T sensors resetting a transistor has been added, and the problem of big capacitance has been solved by a source follower transistor.

By resetting transistors, the horizontal line of pixels are discharged after reading the data. Recently scientists tried to optimize the (3-T) model to (2-T) in order to have less noise (Brouk *et al*. 2008).APS is one of the most commonly used for fabrication till now. Figure 4 shows the (2-T) and (3-T) model diagram.

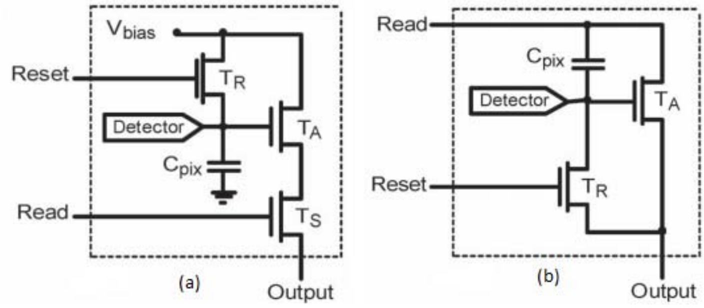

Fig. 4: (a) 3-T model (b) 2-T model (Aghibakhsh and Karim, 2008)

In (4-T) APS, the structure of the transistors has been used as a pinned diode, which gives a floating diffusion node and transfer gate. Extra transistor is used to supply buffering of signal in order to increase the speed of reading data and signal noise ratio (SNR). Reset transistor is used to expand the dynamic range of the sensors as well (Zheng*et al*. 2011).Figure 5 shows the schematic of APS.

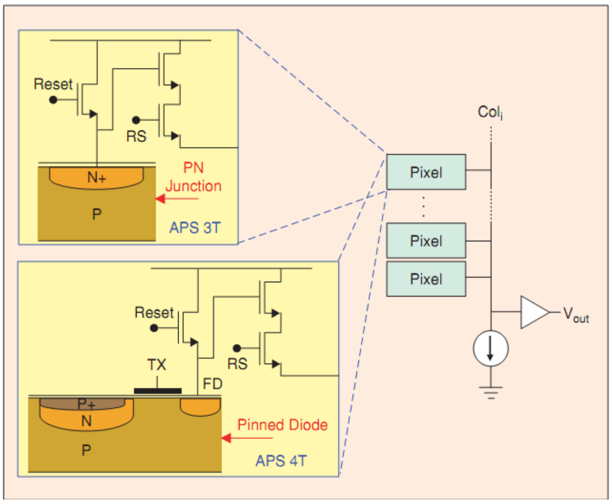

Fig. 5: (4-T) and (3-T) active pixel sensor (APS) (Gamal, 2005)

Pinned Photodiode (PPD):

PPD reduced the dark current noise by collecting the photons of the surface. In order to reduce the noise, the integration node and sense node are separated. In PPD, the photons are collected below it. After that the collected charge is sent to reduce transistors. Figure6 shows the diagram of pinned diode.

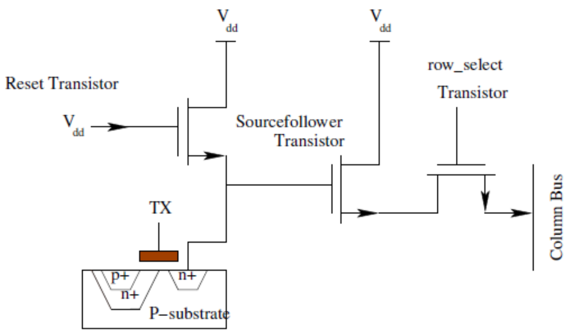

Fig. 6: Diagram of pinned diode (Palakodetyand Saraju, 2007)

Normally PPD uses four transistors with five control line. In this kind of pixels, the number of electrons that collect the blue color is increased so it that it can have an important factor to remove the dark current. In a PPD, absorbed photons are converted and then reset transistor resets the readout node after the illumination. In this level the first calculation of output voltage is done.The collected charge of the photodiode is transferred to the readout node and the photodiode is discharged.After transferring, the output voltage is calculated again.These two calculations are subtracted from each other.

Although PPD has lots of advantages, some disadvantages also exist indeed.It has complex structure as it has four transistor and five lines for controller which make pixels big. It is obvious that it is very difficult to make it smaller than 3µm.According to advantages and disadvantages, it is still preferred to be used in CMOS.

Digital Pixel Sensor(DPS):

The third generation of pixel sensors are the DPS, which consist of photo detector block, ADC unit and memory block in order to reduce the size of pixel in ambulant imaging that was one of the most problems of (3-T) and (4-T) APS. In this case the ADC and memory units have been added to the pixel block (Kitchen 2005). Figure 7 shows the diagram of DPS.

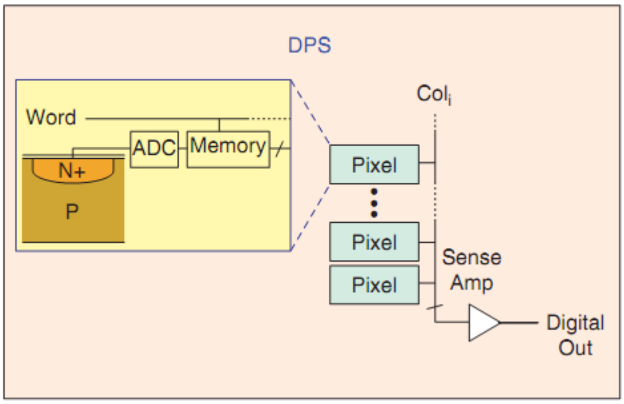

Fig. 7: DPS diagram

Among these sensors, APS and DPS are more useful than PPS. It has been mentioned before that these sensors are unaffected by noise less than PPS. APSs have high consumption in detectors.The only problem of these detectors is the high dark current. In the case of (4-T) pixel, researchers have done some investigation regarding diode size floating diffusion node capacitance and pixel, deep P-Well layer affectation, diversion of epitaxial layer resistivity to reduce the noise and increase the sensitivity. The main points in pixels are low noise and high sensitivity where the charge is collected. In this technology, P-MOS and N-MOS have been used to achieve these issues and the structure of pixels has been changed as shown in Fig.8.

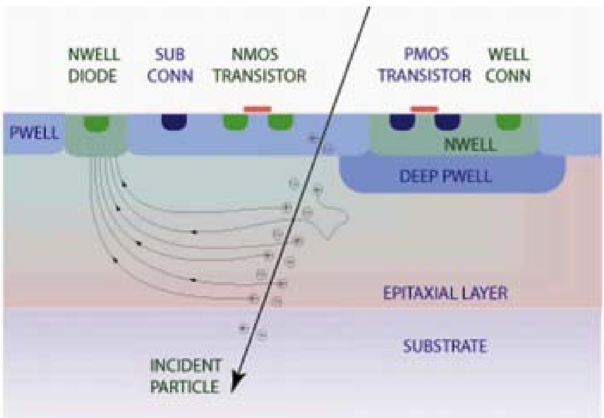

Fig. 8: P-MOS and N-MOS is used (Kitchen*et al*. 2005)

There are many ways to improve the functions in (3-T). One of the latest improvementis the INMAPS which is a kind of detector with the size of 0.18µm. It has the advantage of less charge collection capability and the disadvantage of crosstalk pixels (Coath *et al*. 2010). For developing the (3-T) APS, there is a way to increase the dynamic range (DR) without using any additional power while the CMOS sensor size is 5.5µm. In CIS there are many important factors for designers such as dynamic range, image quality and frame rate. These are influenced by noise of the detector to reduce the noise. The main thing is to increase the dynamic range which is measured by decibel (dB) and the formula is shown in Equation (1).

$$\mathrm{DR(dB)} = 20\log\frac{\mathrm{I_{max}}}{\mathrm{I_{min}}} \quad (1)$$

where I_{max} is maximum and I_{min} is minimum of exposure detection.

For increasing the dynamic range, there are numerous researches. Most of the researchers tried to change the structure of the detectors. Themain problem was the power consumption of these detectors. Recently, there was a research to increase the high dynamic range without increasing the power consumption with this method.

The first method uses a small sensor by size of $5.5 \times 5.5\ \mu m^2$ pixel. To improve the dynamic range, an extra circuit needs to be added so that the space of the photodiodes is increased. Hence the fill factor is increased too. On the other hand by increasing the size of photodiodes the amount of capacity is increased. Thus, more carriers are stored and sensitivity is improved. Double photodiode pixel is one way to achieve this issue that has this advantage. First of all, it influences on photocurrent and makes it counterbalance. In the same way, the current is linear into the light intensity. Figure 9 shows the schematic of photodiode pixel.

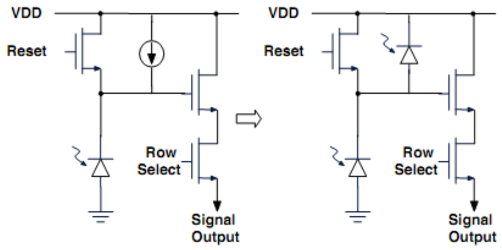

Fig. 9: Double photodiode pixel circuits (Tsai and Wang, 2000)

The source current of the (3-T) pixel is replaced by another photodiode. With this change, the output current will be linear to have a better dynamic range [10].The second method is to use NMOS transistor as a switch to collect the charge which is created by the illumination. Figure 10 shows the diagram of switching transistor which is used in the pixel.

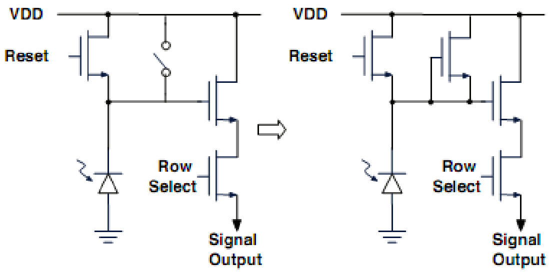

Fig. 10: Schematic of charge collector pixel (Tsai and Wang, 2000)

In the NMOS transistor of Fig. 10, the gate and source are connected together which behaves like a variable resistor switching. When $V_G - V_S = 0$,the resistivity of the layer between gate and source will be changed to high.So, small region between gate and drain is reversed when the photodiode absorbs the photons. The inversion region is changed to thick. Therefore, the resistivity between source and drain become low and the charge that collected by the photo detector can be discharged to the V_{DD}.This charge is more than the illumination (Tsai and Wang, 2000).

As mentioned before, the noise and dark current are two important factors for pixels in order to reduce them. There are lots of methods discussed below.In order to increase the function and performance of CIS, analog signal processing is used. However, they have problems.To solve this, at first,traditional signal processing circuits are located at the edge of the array which avoids the temporal and fix pattern noises (FPN) for illustration correlated double sample (CDS) or double difference sample (DDS) (Yonemotoand Sumi, 2002). Another improvementis increasing the SNR (Nair and Raj, 2000). Signal processing systems are used in the determine applications. K-winners-take-all is a good illustration which can be used in 3-D vision systems,motion detection and improvement of dynamic range (Sekerkiran and Cilingiroglu, 1999).

There are lots of ways to read out data for special applications and these parameters can affect on the performance of the sensors. For example, APS architecture can completely cover high dynamic range and fixed detector bias parameters. However, linearity and pixel size are problems in this kind. While PPS is small enough but does not have good linearity, stable detector bias, good efficiency and high dynamic range (Shih and Wu, 1999). There are also some proper read out methods, such as high sensitivity focal plane array, x-ray capturing and wireless medical imaging systems.

Noises In Image Sensors:

In low light level and multimedia applications, there are two types of noises which is reduces the performance of the sensor. These are temporal noise and fix pattern noise (Schanz *et al*. 2000).

Temporal noise:

It can be divided into different types of noise depending on its source. Pixel noise, photon shot noise, reset or kT/C noise (which is the thermal noise resulting from resetting after each pixel's readout. The k is Boltzmann's constant, T is the absolute temperature; and C is the junction parasitic capacitance), dark current shot noise and MOS device noise (thermal, 1/f or flicker, etc). Column amplifier noise, programmable gain amplifier noise, ADC noise overall temporal noise, noise floor or reading noise are ways to reduce the noise.

Fixed Pattern Noise (FPN):

FPN also called no uniformity is the spatial variation in pixel output values under uniform illumination due to device and interconnect parameter variations (mismatches) across the sensor.FPN consists of offset and gain components which increase with illumination, but causes more degradation in image quality at low illumination.FPN does not change as a function of time and can be characterized assuming a linear pixel response as a variation in the offset and gain at each pixel as shown in Equation (2).

$$V_{ij}(t) = G_{ij}X_{ij}(t) + O_{i,j} \tag{2}$$

whereV output,G gain of pixel,X input,O offset of pixel,Gain FPN pixel to pixel variation of,G_{ij}Offset FPN pixel to pixel variation of $O_{i,j}$.

CMOS (PPS and APS) sensors have higher FPN than couple charge devices and suffer from column FPN, which appears as (stripes) in the image and can result in significant image quality degradation. To find out the sensitivity of the sensors, a high gain column amplifier is necessary to analyze the metal oxide semiconductor. Pinned photo diode is used to decrease the dark current noise and low reset noise. The CDS is the descent FPN and also amplification noise(Kumar *et al*. 2007).

Advanced Generation Of Cmos Images:

There are lots of researches to improve the dynamic range, sensitivity, fill factor,noise and power consumption. With the endeavors of the researchers, there are some improvements.

High Dynamic Range (DR):

Dynamic Range (DR) in one of standard for image sensors which usually use as a ratio to measure the maximum signal to the ground noise with considering about dark condition. DR can restrict by the noise floor times of collection of photons and pixel size. Although, photons collection time can reduced the dynamic range, different illumination or collection time can improve dynamic range read out. By using logarithmic read out, CMOS images can be as efficient as 140dB (Schrey *et al*. 2002). However, there are some disadvantages in logarithmic read out such as high FPN.

In order to improve the DR in the pixel, CMOS pixels logarithmic are produced.The only disadvantages of these pixels are high level of FPN.There have been lots of researches to decrease the FPN.In University of Heidelberg, logarithmic were produced that had a small FPN (Hauschild*et al*. 1998). In 2000, FPN is reduced by new technique reported by Kavadias(Kavadias *et al*. 2000).Kavadias method used APS architecture. The DR was increased to 120dB and the FPN was reduced to 2.5%. After three years, a multi resolution structure was produced which had high DR and low FPN together with low illumination. The latest generation of logarithmic APS is reported in 2010. In this method, with innovation the dynamic range was improved by changes on P-MOS and N-MOS layer of the pixel (Coath *et al*. 2010).

Time-based CMOS Image Sensor:

In order to increase the DR of the pixels, a determined time is used when the voltage of photo detector is decreased less than the time-varying threshold. In the previous image sensors, the DR was limited to the voltage change of the photo detector. There are two clear way for increasing the DR. One of them is the decreasing ground noise and the other one is increasing the power supply. But these methods are not useful for CMOS.

On the other hand, if the read outtime is high, the brighter transistors are saturated. If the time is short, the darker pixels are covered by noise. In each pixel, the voltage of photo detector will be compared byV_{ramp}. When $V_{ramp} > V_{photodetector}$ then data is stored in the eight-bit memory. In DSPs, only one converting cycle of ADC is needed for all pixels that cause to increase the frame rate.Figure 11 shows the schematic of DSP. The output voltage of each pixel is digital but no digital converter is needed.

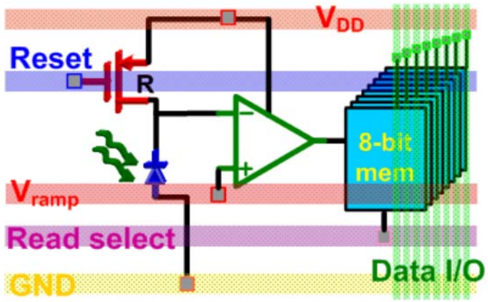

Fig. 11: Schematic of DSP

Time toFirst Spike (TTFS):

Time to first spike (TTFS) overcomes the problems of time-based designs. It can transform illumination into pulse and work in certain time.There is a signal which can occur at the beginning of the every frame and causes brighter pixels. Every pixel has a firing time which can reconstruct the previous scene.

Linear:

Another readout method that can improve FPN in CMOS images called linear readout method.However, their DR is less than logarithmic method.In 1999, a digital CMOS images was produced with high dynamic range with the resolution 1280×1024 (Shih and Wu, 1999). The readout was linear and FPN was low with 69dB DR. In the following year CMOS image sensors was used for automations proposes (Schanz *et al*. 2000). The DR reached 120dB with high image quality and was stable till $85^{o}c$ with linear readout. After two years another technology called spiking pixels pixel level ADC and linear characteristics was proposed(Doge *et al*. 2002). DR was approximately 93dB in that method. In the latest technologies, the linear readout was improved in order to reach better DR and reduce the FPN [26].

High Fill Factor (FF) or High Sensitivity:

FF is the proportion of light-sensitive area to the pixel total size and commonly known as quantum efficiency. It is the proportion of the electrons which is generated in the pixel to the photons of whole pixels area.The image quality is influenced by the number of detectors in the cheap area.As such, the image quality is dependent on FF. There are some limitation in APS CMOS asthe readout circuit reduces FF to 30%. There are lots of research to increase the FF. One of the most common methods is to increase the pixel size. Some lenses help the photons to absorb better on the pixel (Fossum, 1997). The matrix transfer imager methods can reach 40% FF. An APS with the 55% FF, 120dB DR and 1.9 voltage consumption was reported (Hasler, 2002). The latest charge mulplication technology can increase the FF noticeably. Shadowing by metals or silicides, collection of photons by the insensitive junctions of the active pixel, relatively small size of the useful photo-sensitive junction and recombination of photo-generated carriers with majority carriers are the limitation of FF as discussed below.

Low Voltage Operation:

CISare able to work with low voltage (Xu and Chan, 2001).In 1995 NASA, worked on APS sensors to decrease the voltage operation of CIS.After three years the first CMOS APS was produced with the 1.8Vconsumption by FhilipWong. But the sensor had lots of problems as CMOS technology was not advanced during that time(Wong at al. 1998).Research on lowering the power consumption in CIS continued till 2003. CMOS sensor with resolution of$176 \times 144$with 550μW at 1.5Vusing micro batteries was reported during this time (Cho *et al*. 2003). With the Pulse Wide Modulation (PWM) technique the CIS reached to 700nW at 0.5V(Hanson *et al*. 2010).

High Speed Capturing:

High speed sensor method have reached to the pick in 2011. In-situ frame technique reached the speed of one million fps. Even high sensitivity light sensor like a single photon detector with the pixel cab be used to get higher frame rate (Eldesouki *et al*. 2011).

GainAdapted Amplifier:

There are many ways to reduce the noise of the readout of CIS. Gain adapted amplifier is one of the technique useful for 3-transistors, 4-transistors and pinned diode pixels. To improve the CDS, the reset level is first read and charged in the column CDS amplifier capacitor. There is a small problem if the first read out sampling is not amplified. To solve this problem a switch is produced to isolate the input capacitor.Figure12 shows the reset sampling of pixel.

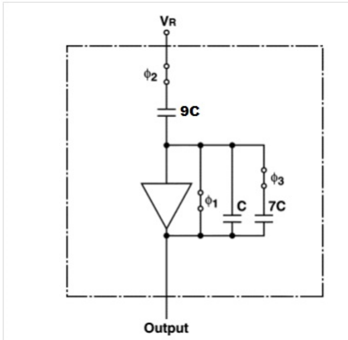

Fig. 12: Reset sampling level (Sakakibara*et al*.2005).

Before the control signal, TX opens the transfer gate of the pixel.The switch controlled by $\emptyset_2$ is turned off to isolate the input capacitor from the pixel output. The other advantage is the level of saturation voltage of the pixel. However, this method uses lots of capacitors and transistors that lead to increase the pixel size. The gain adaptive amplifier used in 4-transistors active pixel sensors is suitable for the quality of the image at low light level.

A Low Noise CIS Read-out Circuit Based on VCO and Frequency Counter:

Recovering accurate timing and delay information in received signals from remote sources is a well-known problem in VLSI signal processing, information and communication systems Voltage controlled oscillators (VCOs) and Phase-Locked-Loops (PLLs) have been the kernel prescriptive solutions to many such problems. Specifically, VCOs have been utilized in any high speed clock recovery systems. Conventional VCO uses analog voltage control for frequency tuning to set up the system. Analog frequency tuning is not compatible with deep CMOS processes. In this method, the analog voltage resolution is unreliable and the analog interface is difficult for integration. DCOs use digital approach for frequency tuning. So, it is easier to implement in advanced CMOS process digital implementation of the PLL loop control circuitry.

Application:

CMOS technology has some advantages such as low power operation, dynamic range and low cost.All these allowsCMOS to be used in lots of application and industrial devices.In addition, astronomy device is one of the common uses of CIS in space.Other devices like robots, star monitoring devices, X-ray satellites, navigation systems, etc. also utilizes CMOS as they are very stable in radiation.

On the other hand in the field of automation CIS can be used in lots of devices like controlling the air bags, precrashdetectors, avertcollision etc. High speed cameras are utilized in intelligent air bags to monitor the situation and decision making [40].CIS can also be used as an assistant and warning system for driver. Figure 13shows the driver assistant's schematic.

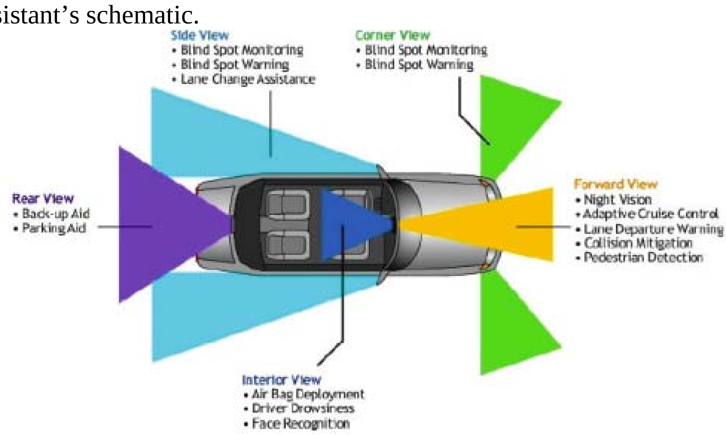

Fig. 14: Schematic of the assistant of the driver(Hertel *et al*. 2008)

In addition one of the usages of CMOS imagers is in medical or biomedical systems which have been developed in 1999 N.Schwarz reported a Retina-implant systems which provide visual sensations to patients suffering from photoreceptors degeneration another request in recent years is to digitize the medial images specially in radiology-ray imaging system with large FOV(field-of-view)using image CMOS sensor has been proposed by Ho Kung Kim , after two years S. Wook Lee investigated on 3-D X-ray microtomographic system, that the inner structure of small object can be seen without ruination (Kim *et al*. 2001).

Nowadays by improvement the CMOS technology and high performance of resolutions the variety of 3-D devices is increased in the field of domestic and industrial proposes, real time systems which need high speed and high resolution can use 3-D technology.3-D range imaging technology or range finder is a technology to measure the deep of material.Time-of - flight(TOF) measurements or interferometry 3D X-ray imaging [41], Robot vision are some devices that use 3-D methods (Kawahito*et al*. 2007).

Discussion:

As mentioned previously, CIShasfew problems which researcher tried to resolve. The three important problems are low dynamic range, high FPN and low power consumption. These problems are related to each other. For example, the dynamic range is increased then the FPN is also increased. In order to improve the dynamic range, some methods are used which make the sensors to increase the dynamic range up to 120dB. These are logarithmic,time based sensors, time to first spike and linear readout. In order to reduce the power consumption, the high dynamic range is decreased respectively. During the decades, researchers tried to make the balance by changing the structure of the pixels, changing the methods of reading data, altering the structure of ADC and adding special circuits to change the amplifier’s gain. PPS was rejected due to high noise affection. APS sensors developed during the years, exist in two transistors models, three transistors model and four transistors model. Each model has its own problems. For example, in four transistor model, the dark current is high. P-well and N-well technique used in the structure of the pixel improved both dark current and also problems in (3-T) by adding pinned diode in that structure.However, the pixel size and device size became large.

CIS made a huge technological progress over the last decade. The introduction of the pinned photodiode really boosted their success. Exploring the typical characteristics, needs and requirements of the imaging application can result in very attractive circuits and devices that increase the performance of the imagers. Because of the ever-shrinking dimensions in CMOS technology, further integration on column level and even on pixel level can make the imagers even smarter than they are already.

Time-domain imagers exhibit a tradeoff between integration time and dynamic-range, whereas the tradeoff with dynamic-range in voltage-domain imagers is with the DC supply voltage. Defining the dynamic range of a time-domain imager as a function of the ratio between the maximum to minimum integration times depends on the dynamic-range required for a specific application. However, time-domain imagers are a good choice when dealing with application that require very high dynamic-ranges (~100 dB) and low-power consumption since they can operate from lower supply voltages compared to voltage-domain imagers.

Conclusion:

CIS made a huge technological progress over the last decade. The introduction of the pinned photodiode really boosted their success. Exploring the typical characteristics, needs and requirements of the imaging application can result in very attractive circuits and devices that increase the performance of the imagers. Because of the ever-shrinking dimensions in CMOS technology, further integration on column level and even on pixel level can make the imagers even smarter than they are already.

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