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Multi Phase Switching Converters with Extended Range Multi-Inputs

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ABSTRACT

The switching converters with single-input, three-phase control circuit, can control three-phase voltage driven dc loads (for example-three-phase dc motor) such that the average voltage applied to each phase of the dc load in each sampling period is proportional to the sampled analog input signal. The existing three-phase control circuit can function for limited range of input signal for single analog input signal. The proposed multiple-inputs multiple-phase control circuit has extended range of input signal and controls the multiple-phase dc loads such that the average voltage applied to each phase of the dc load in each sampling period is proportional to the product of the sampled multiple input signals. The multi-inputs multi-phase control circuit shall find application in the industries with custom made multi-phase dc loads that are demanding very high power and at the same time each phase voltage is needed to be controlled by the product of multi-variables.

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INTRODUCTION

In switching converters (SCs) average dc output voltage must be controlled to a desired level and is proportional to switching control signal. SCs use one or more switches to transform dc from one level to another. In a SC, with given supply voltage, average output voltage is controlled by controlling the on and off durations of a switch. The property that Delta-Sigma modulator (DSM) output can directly drive bridge type SC is made use in the proposed SCs.

The single-input three-phase SC, based on conventional DSM with hexagonal quantizer improves SNR but range of input signal is limited to 60% of supply voltage (Glen Luckjiff and Ian Dobson, 2005). In (Jonathan, W. et al., 2010) is proposed a new control method for the multi-phase high frequency conversion. The method combines conventional digital control, Delta-Sigma Modulation and VHF conversion techniques. The results show a non-linear but monotonic input to output characteristics. The application of DSM for the voltage regulation in multi phase driver is analyzed in (Prieto, J., et al., 2009). The method is simpler than Space Vector Pulse Width Modulation (SVPWM) method but the range of input signal is limited to 60% of full scale. The Research papers (Glen Luckjiff and Ian Dobson, 2005; Jonathan, W. et al., 2010) and (Prieto, J., et al., 2009) operates on single analog input signal and generates three/multi phase voltage.

In the proposed multi-input multi-phase SC, multi-phase voltage is generated and each phase voltage (for example voltage applied to multi phase dc motor) is proportional to product of multiple analog input signals. Each phase voltage leads by 360 °/n (where n is number of phases a, b, c etc. in phase sequence a-b-c etc. The output from most of the safety devices/circuits is binary. The multiplication of the outputs of these devices along with control signal automatically nulls the input control signal when the system is not safe. In the proposed DSM based SC new type of vector quantizer is proposed and the dynamic ranges of input signals can go up to 90% of supply voltage.

Design Of Multiplier With Two Inputs:

The block diagram of multiplier for two inputs MUL2 (Diwakar, K., C. Senthilpari, 2009) is shown in Fig.1(a). The unit D represents a delay of one clock period. The first sample and hold circuit (S/H1) samples the input signal *analog x* at a sampling period T_U. The sampled analog input signal x is fed to input of DSM1. The DSM1 circuit is operating with clock of period T_C ($T_U >> T_C$). The SR flip-flop is reset (phase Φ_{OFF}) during each positive transition of clock signal. The output of single bit quantizer, Q_1 is in 1 state or in 0 state. When the quantizer output is in 1 state, SR flip-flop is set (phase Φ_{ON}).

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The second sample and hold circuit (S/H2) samples the input signal *analog y* at a sampling period T_U. The DSM2 circuit is also operating with clock of period T_C. The sampled analog input signal *y* is fed to input of DSM2 during phase Φ_{ON}. The variable *y* is negated and fed to DSM2 during phase Φ_{OFF}. During each sampling period, the bit stream at the output of quantizer Q_2, gives digital representation of product of sampled input signals. The average value of bit stream at the output during each sampling period (*z*) gives the analog value of product of normalized samples of input signals ((x/n)×(y/n)) where *n* is feedback gain. Therefore, normalized value of *z* (*nz*) is equal to normalized product of input signals (*xy*/*n*). The input signals can be increased up to ±90% of supply voltage which is the feedback gain (n).

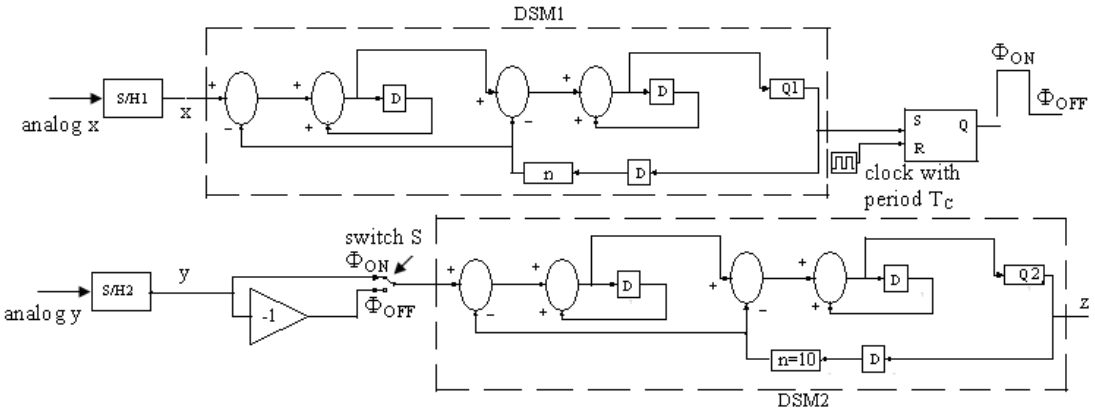

Fig. 1(a): Proposed multiplier with two inputs.

The multiplier with two-inputs can be extended for multiplication of multiple inputs. In Fig.1(b) is shown the method of extending two-input multiplier for multiplication of three inputs (MUL3). The output of MUL2 is in 1 state or in 0 state. When MUL2 output is in 1 state, SR flip-flop is set (phase Φ_{ON}). The third sample and hold circuit (S/H3) samples the input signal *analog z* at a sampling period T_U. The DSM3 circuit is also operating with clock of period T_C. The sampled analog input signal *z* is fed to the input of DSM3 during phase Φ_{on}. The variable *z* is negated and fed to DSM3 during phase Φ_{OFF}.

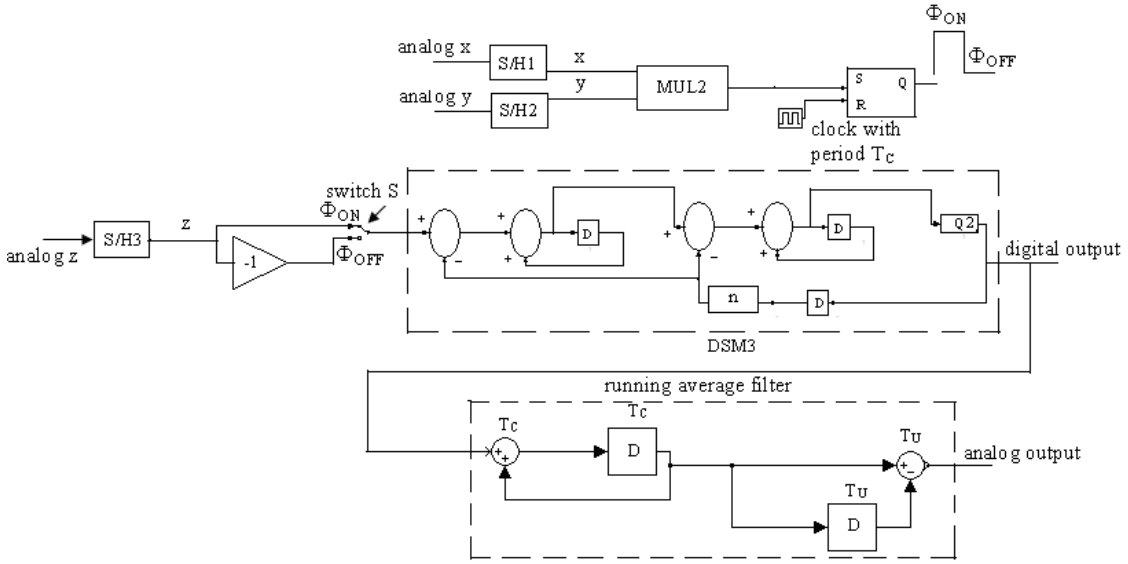

Fig. 1(b): Proposed multiplier with three input signals(MUL3).

During each sampling period, bit stream at the output of quantizer Q_2, gives the digital representation of product of sampled input signals. The average value of the bit stream at the output during each sampling period gives the analog value of product of normalized samples of input signals{(x/n)×(y/n)×(z/n)}.

Proposed Vector Quantizer:

In scalar single bit quantizer, the quantizer input x_q is quantized to +1 when x_q is any positive value or zero.

The quantizer input is quantized to -1 when x_q is negative. The idea of scalar quantization is extended to vector quantization. The proposed vector quantizer for six phase generation is shown in Fig.2(a). The circle of radius $(x_q)_{max}$ is divided into twelve equal sectors. The vector falling in any sector is represented by representative vector in each sector. Each representative vector bisects the corresponding sector and its magnitude is 1. This idea can be extended to any multi-phase generation. The conventional six phase switching circuit (custom made power circuit) is shown in Fig.2(b). The supply voltage is $\pm V_S$ and some phase circuit use the tapings from $\pm V_S$ as supply voltage. The switching circuit has twelve switching states corresponding to twelve output vectors of proposed vector quantizer. Q_1 to Q_{12} are solid state switches. The output of switching circuit (a,b,c,d,e,f) drives balanced six phase load like custom made six phase dc motor.

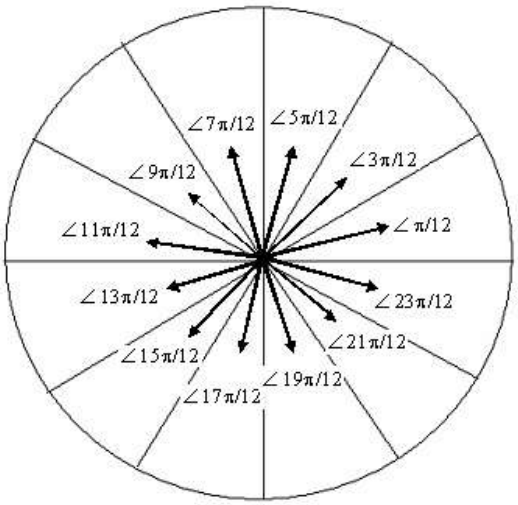

Fig. 2(a): Proposed vector quantizer for six-phase control circuit. (Magnitude of all vectors=1)

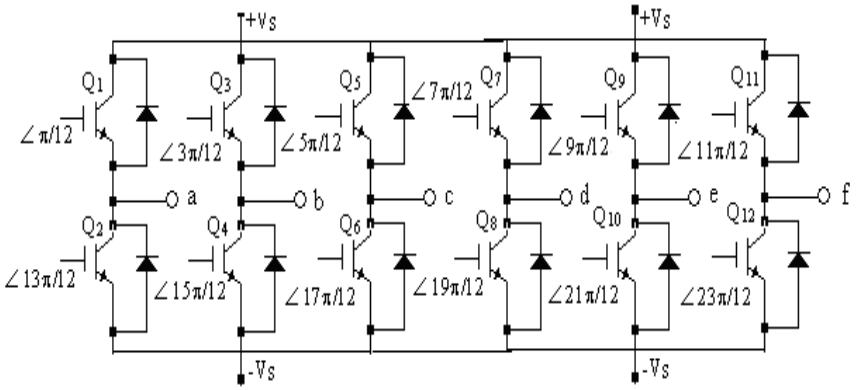

Fig. 2(b): Six-phase switching circuit.

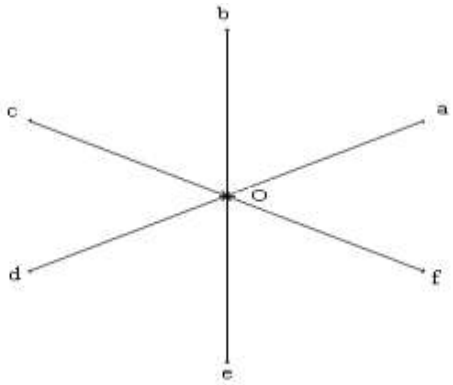

Fig. 2(c): Connections to armature windings of six-phase dc motor

The armature windings of the custom made six-phase dc motor are placed at equidistant angle of 60°. The outputs (a to f) of six-phase switching circuit is connected to armature windings as shown in Fig.2(c).

Block diagram of proposed four-input six-phase SC:

As an example of multiple-input multi-phase SC, the block diagram is presented for four-input six-phase

SC and is shown in Fig.2(d).The sample and hold circuits (S/H1 and S/H2) samples the input signals at a sampling period T_U. The analog input signal to S/H2 is the analog signal from output of proposed three input multiplier. The analog signal to S/H1 is the fourth analog input signal. The sampled fourth analog input signal, α is fed to input of DSM. The sampled second input signal β is used to control operating period of DSM. The DSM circuit is operated by clock with period T_C ($T_C << T_U$). The feedback gain is equal to n (10) which is supply voltage of circuit. Therefore, dynamic range of α and β is 70% of feedback gain (-7 to +7). During a positive transition of update signal, SR flip-flop is set. When SR flip-flop is set (phase Φ_{ON}), switches s_1 to s_7 are closed (shown by thin dotted lines) and DSM starts functioning.

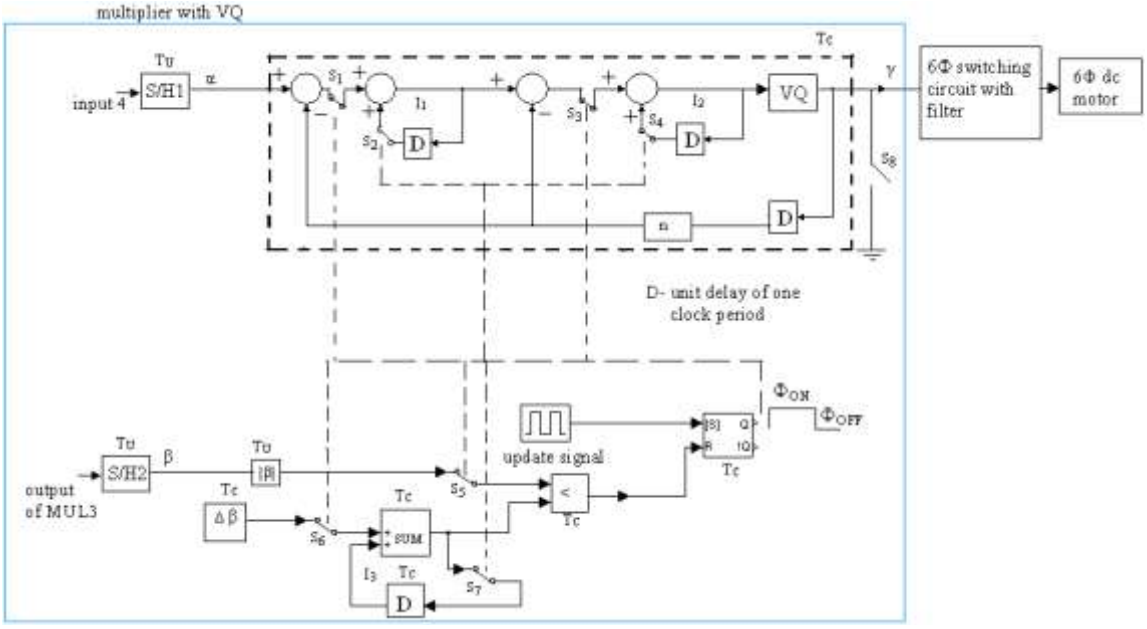

Fig. 2(d): Proposed six-phase SC with four input signals.

The resolution of DSM output, Δγ is given by, $\Delta\gamma=T_C.n/T_U$. The resolution, Δγ is integrated when the R-S flip-flop is set. The integral value of Δγ, $(\Delta\gamma)_{cum}$ is compared with |β|. When $(\Delta\gamma)_{cum}>|\beta|$, SR flip-flop is reset (phase Φ_{OFF}). The switches s_1 to s_7 are opened, the DSM stops functioning and output is zero for remaining sampling period since quantizer output is clamped to analog ground through switch s_8. All the integrators, denoted as I_1, I_2, and I_3 are reset to zero and cumulative addition of Δβ also stops. The value of Δβ is selected in such a way that in a sampling period, $(\Delta\beta)_{cum}$ never exceeds maximum value of |β| which is equal to n. When β is negative quantizer output is inverted (not shown in figure) to get correct sign for product, αβ. During next positive transition of update cycle, DSM operating cycle is repeated. There are twelve outputs from the vector quantizer ($1\angle\pi/12$, $1\angle3\pi/12$, $1\angle5\pi/12$, $1\angle7\pi/12$,$1\angle9\pi/12$,$1\angle11\pi/12$, $1\angle13\pi/12$, $1\angle15\pi/12$, $1\angle17\pi/12$, $1\angle19\pi/12$) and values of outputs depend on which sector quantizer input falls. For example, the output $1\angle\pi/12$ represents a pulse of unit amplitude with a phase angle $\pi/12$. When the output of quantizer is $1\angle\pi/12$, switch Q_1 will be closed.

The multiplier circuit with vector quantizer gives the six-phase output such that magnitude of each phase voltage is equal and proportional to product of samples of input signals. Each phase voltage leads by 60 ° in phase sequence a-b-c-d-e-f. The six phase power circuit with running average filter in each phase drives six phase load, proportional to product of input signals in both directions. The voltage applied to each winding of custom made six phase dc motor is proportional to product of sampled four analog input signals in each sampling period.

Simulation Results:

The simulation is done using Matlab Simulink. In Fig.3(a), the first three waveforms show three input signals to proposed multiplier. The fourth waveform shows the analog input signal which is fed to S/H1 of Fig.2(d). The normalized average value of quantizer output of Fig.1(b) during each sampling period (nz) is shown as fifth waveform in Fig.3(a) and is proportional to product of normalized samples of the first three waveforms (x/n, y/n, z/n) in each sampling period.

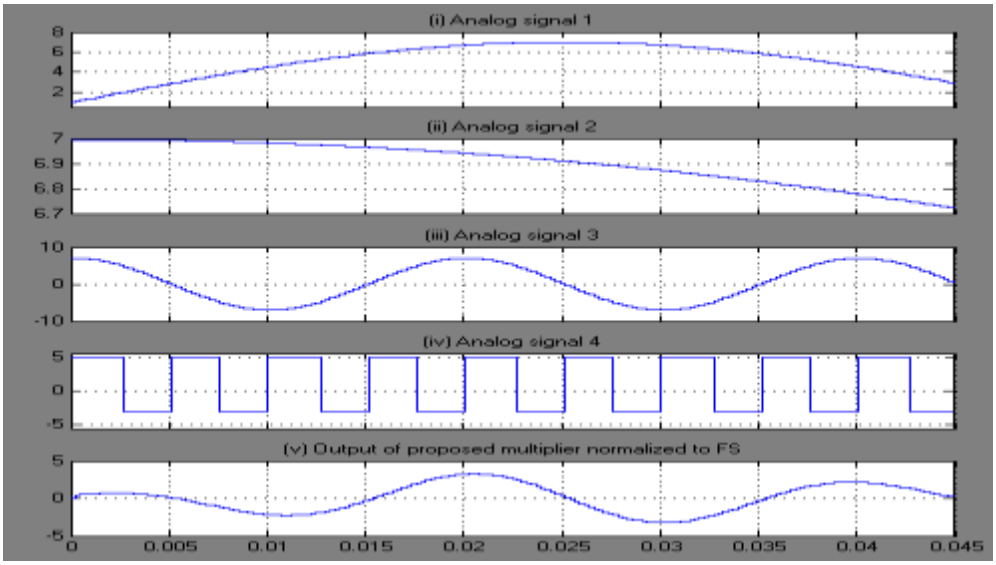

Fig. 3(a): Functioning of proposed multiplier with three inputs (Horizontal axis- Time in sec., Vertical axis- Voltage in volts).

The proposed multiplier and the proposed six phase SC are simulated with T_U=2.442 msec and T_C=0.1μsec. Fig.3(b) shows magnitude of six-phase (a-b-c-d-e-f) output of vector quantizer of Fig.2(d). The magnitudes of phase voltages are equal and proportional to product of four sampled analog input signals. Fig.3(c) shows phase angles of six-phase (a-b-c-d-e-f) outputs of the quantizer (Horizontal axis- Time in sec., Vertical axis- Angle in radians). The outputs lead by 60° in the phase sequence a-b-c-d-e-f. The phase angles are 0,π/6, 2π/6,3π/6,4π/6,5π/6.

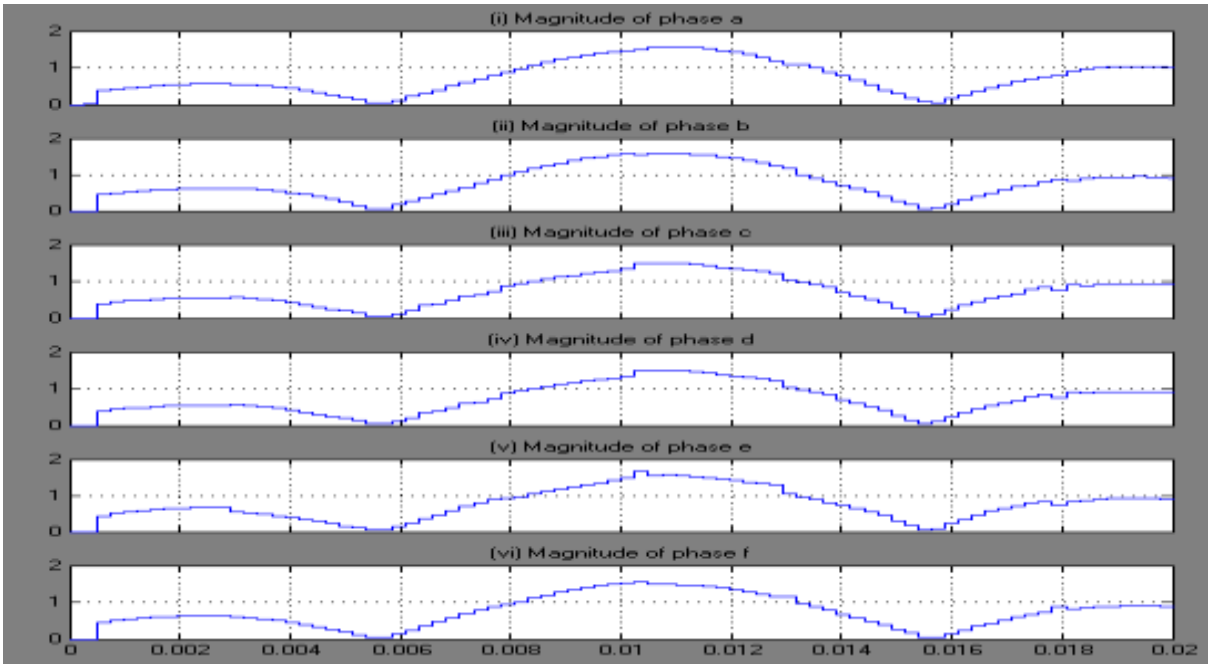

Fig. 3(b): Magnitudes of six-phase voltages of proposed SC with four-input signals (Horizontal axis- Time in sec., Vertical axis- Voltage in volts).

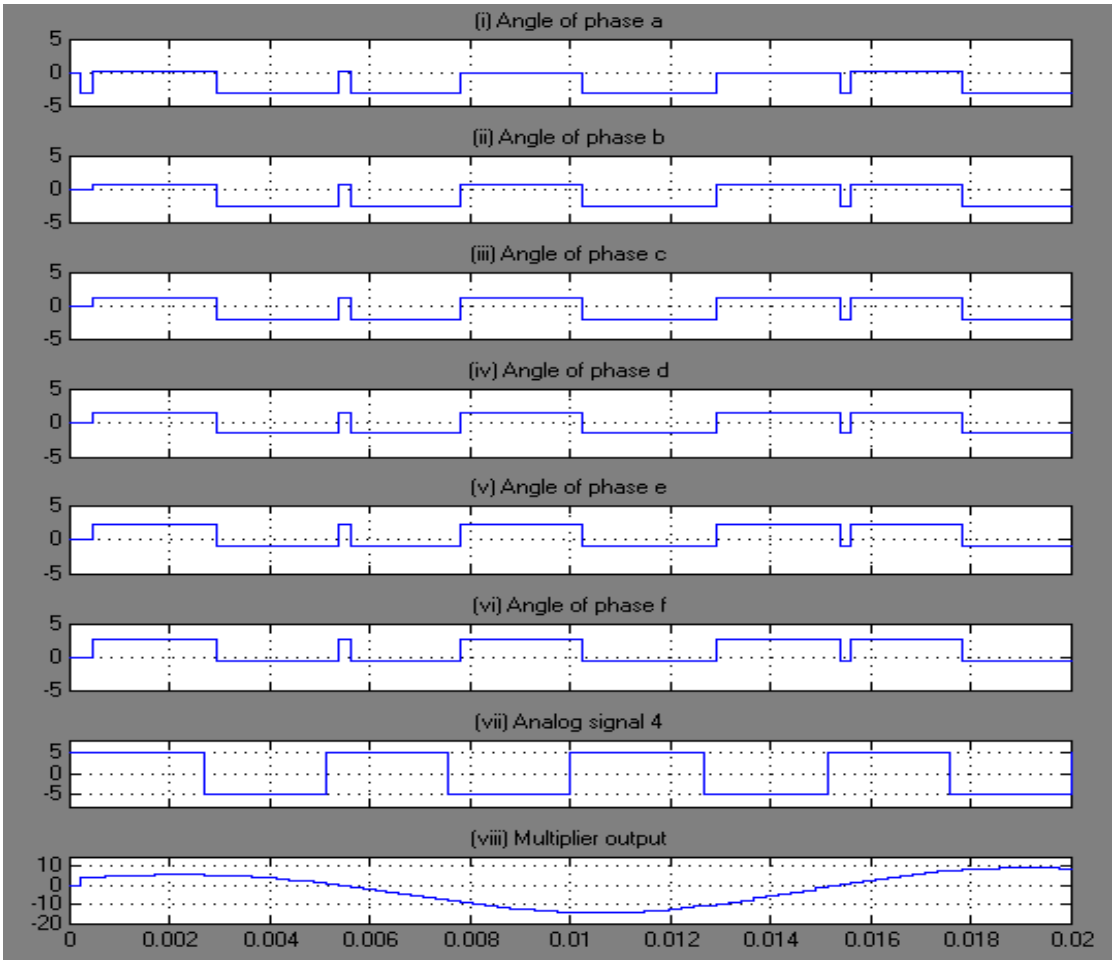

Fig. 3(c): Phase angles of six-phase voltages of proposed SC with four-input signals

(Horizontal axis- Time in sec., Vertical axis- Angle in radians for (i) to (vi) and voltage in volts for (vii) and (viii)).

Conclusion:

The proposed multiple-inputs multiple-phase control circuit controls the multiple-phase dc loads such that the average voltage applied to each phase of the dc load in each sampling period is proportional to the product of the sampled multiple, extended range of input signals. The multi-inputs multi-phase control circuit shall find extensive application in the industries with custom made multi-phase dc loads that are demanding very high power and at the same time each phase voltage is needed to be controlled by multi-variables.

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