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Soft-Error-Resilient LDPC Architecture on SoC Using NoC Decode Algorithm

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ABSTRACT

The design process in wireless technology needs more effort in flexiblity and throughput equipments. The existing design mainly focuses on the baseband processing units in wireless transceivers. By increasing the flexibility of WiMAX will leads to soft-error, which degrads the performance of the transceiver. The proposed work is designed by concerning Network-on-Chip (NoC) based LDPC decoder architecture. And this proposed work concentrates first on improving the throughput by exploiting flexible LDPC error-correction technique. This Flexible LDPC decoder design is reliable for both single-bit binary and multi-bit binary. By modifying the functionality of a router with LDPC algorithm using NoC, the router is enabled to establish the reliable communication without an error. And communication is established based on the information given in the header of the packet. The LDPC algorithm is implemented by involving Bit-node and Check-node. And process is implemented by Tanner-graph implementation by involving forward and backward recursion. Moreover, synthesis results show that the proposed design can offer high throughput for WiMAX by supporting the whole set of flexible LDPC decoder. With this technique we can improve the throughput more than 100 MB/s.

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INTRODUCTION

In wireless communication throughput is increased by increasing the flexibility of the architecture (Tenhunen, J.H., 2003). This flexibility creates the challenging issue, one of the challenging issue is soft-error. The soft-error is an error which will create the malfunction due to the leakage of current or voltage (Berrou, C., 1993). There are two steps used to solve this issue, one is error detection which is done by parity bits and another one is error correction which is done by LDPC decode algorithm (Dally, W.J. and B. Towlesm, 2001). The communication establishment is done with the information given in the header of the packet (Charles, R.K.J., 2013). The main aim of designing LDPC in wireless communication is to employ high-throughput and flexible error-correction. The requirement for error-correcting in NoC adds more issues such as error-detection, ability to find and locate errors, and designing an error-free network. With LDPC decoders high throughput is achieved by performing parallel process, where all processing elements (PEs) perform the decoding process concurrently on the different portion of the received frame (Zitouni, A., 2006). But using LDPC, PEs requires a large bandwidth for efficient interconnection of concurrent read/write data from/to the memory (Nandhini, R. and N. Devarajan, 2014). Generally, error-detection and correction can protect the system from transient errors in communication subsystem. The proposed work is done in two folds (i) the design of intra-IP based-NoC by flexible LDPC decoding with the clear design flow (ii) Flexibility achieved through intra-IP-NoC based approach is proved. For proposed work, consider the standard WiMAX standard architecture has worst-case throughput. While transmitting the packet, the sender adds error detection codes (parity code) in the packet, and receiver check the received data for error-correction (Alles, M.T., 2008). The messages are transmitted continuously from sender to receiver using cut-through switching, without waiting for an ACK. If any error is detected in the data, it is recovered in LDPC decode algorithm using bit-node and check-node (Helali, A., 2006). Finally the error-corrected data is sent to the receiver. The proposed LDPC algorithm is implemented with Bit-node and Check-node, where bit-node process in d_p, elementary steps and check-node process in d_c (d_c-1) elementary steps whereas d_b and d_c denotes the bit-node and check-node degree respectively. But for an efficient implementation the process of check-node is complex, when check-node degree is high (Murugappa, P., 2011).

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Australian Journal of Basic and Applied Sciences, 8(18) December 2014, Pages: 106-111

And the comparison about error-recovery is made for different Network-on-chip architecture. Section II and III deals with NoC interconnection architecture and PEs, Experimental results for WiMAX are shown in section IV and conclusion are shown in Section VI.

2. LDPC Decoding Algorithm:

The LDPC decode algorithm performs iterative method based on message-passing and data-passing phases. And throughput is increased by its flexibility for one-bit and two-bit. LDPC codes are characterized by sparse *MxN* parity check matrix *H*, and codewords *x* satisfies $H.x^T=0$, compose of zero and Non-zero bits as represented in Eq 3.1.And each code is represented by Tanner graph, which contains two sets of nodes : Bit nodes and Check nodes.

$$\begin{pmatrix} 1&0&0&1&0&0&1&0&0 \\ 0&1&0&0&1&0&0&1&0 \\ 0&0&1&0&0&1&0&0&1 \\ 1&0&0&1&0&0&1&0&0 \\ 0&1&0&0&1&0&0&1&0 \\ 0&0&1&0&0&1&0&0&1 \end{pmatrix} \cdot \begin{pmatrix} y_1 \\ y_2 \\ y_3 \\ y_4 \\ y_5 \\ y_6 \\ y_7 \\ y_8 \\ y_9 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \quad (1)$$

Bit-nodes are associated to the *N* bits of code-word, whereas check-nodes corresponds to the *M* parity-check constraints.

The parity check matrix in LDPC has constants W_c non-zero bits in each column and constant W_r non-zero bits in the each row, where $w_r=w_c (w_n/w_m)$. If the non-zero bits in each row and column is not constant and the parity check matrix *H* is also low density then the code is an irregular code (Viswanathan, N., *et al*., 2012) And the corresponding parity check matrix is represented by Tanner Graph in Fig.1.

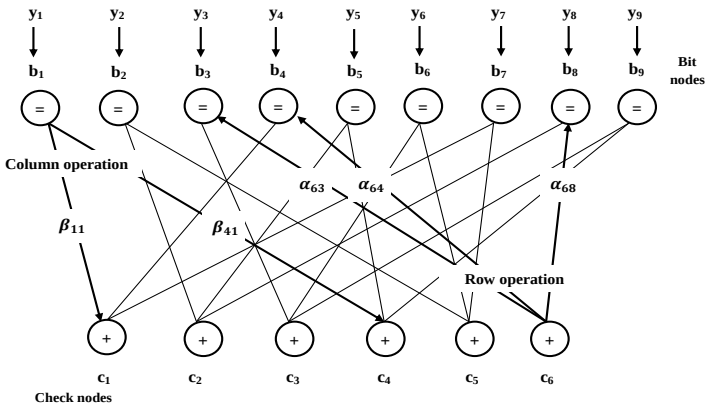

Fig. 1: Parity Check matrix tanner graph.

The received code in the LDPC is decoded iteratively, using the message-passing algorithm. The received code is evaluated from each bit, where evaluation is done at each row of the parity check equations corresponding to the check node. In the message passing algorithm column index sets *A(m)* and row index sets *B(n)* are defined as follows

$$A(m) \triangleq \{n|H_{mn} = 1\} \quad (2)$$

$$B(n) \triangleq \{m|H_{mn} = 1\} \quad (3)$$

Where the conditional probability for $x_i = 0$ and $x_i = 1$ is explained as follows

$$P(y_i|x_i = 0) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{(y_i-1)^2}{2\sigma^2}\right) \quad (4)$$

$$P(y_i|x_i = 1) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{(y_i+1)^2}{2\sigma^2}\right) \quad (5)$$

The steps involved in error detection and correction are explained below

Step 1: Initialization

The LLR computation equation for λn is shown in equation 5.4 where n varies from 0,1…..N.

$$\lambda_n = 2y_n/\sigma^2 \quad (6)$$

Where σ^2 is the variance of noise and $\beta_{mn} = \lambda_n$ for each *(m , n).*

Step 2: Row operation

Australian Journal of Basic and Applied Sciences, 8(18) December 2014, Pages: 106-111

For all check node $c_{m,}$ corresponding to m=0,1….M computes the intermediate messages α_{mn} with the following equation

$$\alpha_{mn} = \left(\prod_{n'\in A(m)/n} sign(\alpha_{mn'})\right) \times f\left(\sum_{n'\in A(m)/n} f(|\beta_{mn'}|)\right) \quad (7)$$

Where *f(x)* is defined as follows

$$f(x) \triangleq \ln\frac{\exp(x)+1}{\exp(x)-1} \quad (8)$$

Step 3: Column operation

For all bit node *bn* corresponding to n=0,1….N computes the intermediate messages β_{mn} with the following equations

$$\beta_{mn} = \lambda_n + \sum_{m'\in B(n)/m} \alpha_{n'm} \quad (9)$$

Step 4: Tentative decision

The tentative LDPC code $\hat{y}_n$ for n=0,1,…..N is given by

$$\hat{y}_n = \begin{cases} 0, & sign\left(\lambda_n + \sum_{m'\in B(n)} \alpha_{m'n}\right) = 1 \\ 1, & sign\left(\lambda_n + \sum_{m'\in B(n)} \alpha_{m'n}\right) = -1 \end{cases} \quad (10)$$

Step 5: Parity Check

If the tentative code word satisfies the following equations, code-word and output exit the message-passing algorithm

$$H.(\hat{y}_1, \hat{y}_2, \dots, \hat{y}_N)^T = 0 \quad (11)$$

Step 6: Increment counter

The loop counter values are set for $l<l_{max,}$ otherwise quit the cut-through algorithm

$$\lambda_n = \ln\frac{P((y_n|x_n=0))}{P((y_n|x_n=1))}$$
$$= \ln\frac{1/(\sqrt{2\pi\sigma^2})\exp(-(y_n-1)^2/(2\sigma^2))}{1/(\sqrt{2\pi\sigma^2})\exp(-(y_n+1)^2/(2\sigma^2))}$$
$$= -(y_n-1)^2/(2\sigma^2) + (y_n+1)^2/(2\sigma^2)$$
$$= 2y_n/\sigma^2 \quad (12)$$

The results show that bit-error rate of data in Memory is reduced by NoC based LDPC decode algorithm. The hardware functions are realized by compensation technique and Look-up tables (LUT). After the packet data leave from the LDPC algorithm, the received packet does not contain any error.

3. NOC Architecture Design:

LDPC have a complex message passing phase, which varies in terms of interconnection and duration of parallel process of the decoder. In this section the NoC design is processed with LDPC support. The NoC architecture is shown in Fig. 2 and structure of nodes is shown in Fig.3. A Network of node is made of Processing Element (PE), Routing element (RE) and Memory (MEM) to store the incoming messages (Guerrier, P. and A. Greiner, 2000). The RE is based FxF crossbar, where it is F input FIFOs and F output registers. The three important things to design NoC is topology, routing mechanism and switching algorithm. The topology defines how to interconnect the nodes in the network and Switch is enabled after receiving the header of the packet that contains the information about the destination address. The switch In switch input channel is connected to the output channel. There are many switching techniques used: store-and –forward switching, cut-through switching and wormhole switching.

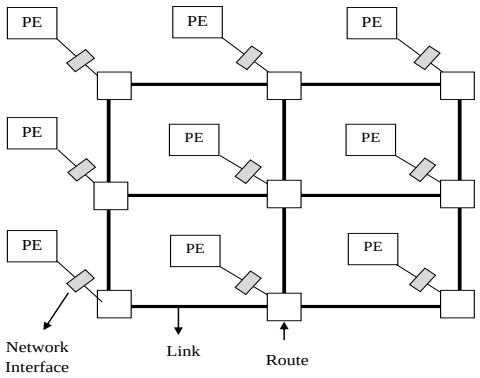

Fig. 2: 2D NoC Architecture.

In our proposed system router is designed with cut-through switching which requires less wires and less number of buffers when compared with other switching. In cut-through switching packets are transmitted continuously by split the packet into flits and header flits contains the details about destination address (Badrouchi, S., 2005). The architecture of node structure is shown in Fig.3. The routing algorithm and network topology are the two important aspects for on-chip communication in NoC. The Router makes the path for the received packet to the destination. The main property of route in NoC should make the path to error-free, deadlock-free and highest performance. The route in the NoC is divided into two parts, one is source node which makes the path before packet leave from the source and another one is the destination route which make the path based on the information given in the header of the packet (Revathy, M. and R. Saravanan, 2014).

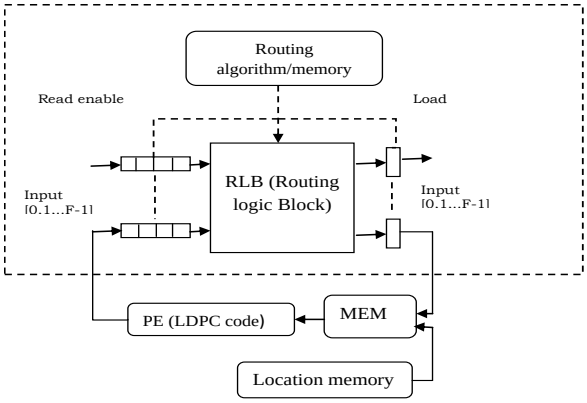

Fig. 3: Node structure.

4. Processing Element Architecture Design in NOC:

To design Processing element for LDPC decoding, it must be designed by standard and support structure with code rates and block lengths (Martina, M., 2000). Fig.4 shows the architecture of PE based on the LDPC core. In the Fig.4 architecture of LDPC decoding are shown with memory, where values are read from memory by storing the incoming messages from the network. In the read/write processor, there is one dedicated memory to store the computed value. Then the received values are sequentially compared with Minimum Extraction Unit (MEU) to find the minimum values (Vimalraj, S.L.S., 2014). Concurrently the values stored in the processor's memory will be in use during the next iteration. This architecture is only limited by the size of the memories and completely independent of the code. Both processing and dedicated memories should have enough storage capacity to manage heavy workload among the supported codes. The synthesis results show that worst case among the given WiMAX codes by parity checks. And performance of WiMAX using LDPC code with NoC is compared with LDPC without NoC, which occupies more area and has the highest throughput.

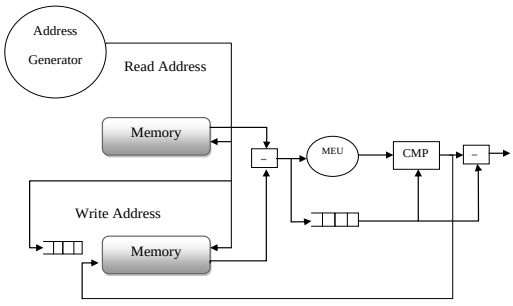

Fig. 4: LDPC decoding core.

5. Error-Correction Mechanism Using LDPC Algorithm:

In the error-detection scheme parity bits are added to each packet. The parity encoder is added to the sender NI and the decoder is added to the receiver NI (Salem, A.K.B., 2010). The sender NI has the one or more buffers to store the packet. After receiving the ACK and NACK signal from the receiver based on the error details the sender will send the packet to the receiver. To account the error at the ACK and NACK at the packets, the sender adds the time-out mechanism with the packets for retransmission (Hocevar, D., 2004). If there are any duplicate packets, receiver identifies it by using packet-sequence detectors, because the header flits contain the information which is protected by parity bits. If any error is detected at the header flit by switch it

drops the packet and requires for retransmission. The performance evaluation of NoC based LDPC decoder is shown in synthesis results. The parity check matrix of the LDPC code is started, once the decoding, scheduling and topology are chosen. The performance analyzes of NoC based LDPC decoder architecture is analyzed from the following design flow

- Initially the definition of graph representation for the *H* matrix is represented. Scheduling is chosen to perform on the size and structure of the graph and on-zero entry present in the same column of both *i* and *j* (Kim, J.H. and I.C. Park, 2009).
- The second step is NoC topology selection, in our design Mesh topology is considered.
- The mapping of the LDPC code problem on the specific NoC is identified in terms of graph and solved using a message-passing algorithm.
- After assigning graph node on the NoC node, the equivalent interleaver is designed for topology.

After this analysis, LDPC check nodes are partitioned among each NoC. The number of clock cycles required for each iteration is analyzed (Faudzi, A.A.M. and K. Suzumorim, 2010).And synthesis is repeated for the several values of the following parameter

- PE output rate: is the number of messages produced by PE in a clock cycle.
- Routing algorithm: Three different algorithms are embedded in the rely, to identify the to identify the shortest path between the nodes by storing the information in one or more routing tables.
- Send/Delay messages: this parameter arises when two or more messages required to the same output port. In this type the first message is routed based on the selected routing algorithm, where colliding messages are kept in FIFO by DCM strategy. If SCM is choosed for the route of non-colliding messages will be configured by treating the colliding messages as "don't care".
- Route local (RL): this flags arises to store the sent and receive messages. If any messages are stored in the router (RL=1) the flag will bypass the routing (RL=0).

6. Results:

Table 1: Throughput Analysis WIMAX LDPC.

Decoder	LDPC with NoC for WiMAX	LDPC without NoC for WiMAX
Tp [nm]	110	90
A_{core} [mm^2]	2.56	3.17
A_{tot} [mm^2]	3.15	3.56
f_{clk} [MHz]	520	400
Pow [mW]	86.2	76.8
DW	9-6	7-5
It_{max}	25	15

With the detailed study, complete design of the LDPC decoder for WiMAX standard has been implemented. By increasing the flexibility of the architecture, it will create the errors, one of the errors is soft-error.The LDPC decoder has been designed at the register-transfer level in Verilog HDL. And synthesis results together with LDPC decoder is shown in Table 1 and the throughput has been computed

$$T = \frac{(N-M).f_{clk}}{(lat_{core} + n_{cycles}).It_{max}} \quad (13)$$

Where f_{clk} is the clock frequency, It_{max} is the maximum number of iterations, lat_{core} is the maximum number of decoding core and n_{cycles} is the duration of message passing phase (Nallathambi, G. and S. Rajaram, 2014). Table 1 results have been obtained with above equation (5.1).And the core area of NoC architecture with LDPC is also shown in Table 1. The complexity in topology is due to the complexity of node (number of messages) in the architecture (Hababeh, I., 2013). But by using LDPC decoder in WiMAX standards, can achieve higher throughput. And it is worth that the characteristic of LDPC decoder, together with memory access will reduce the power.

Discussion:

The WiMAX designed to increase the performance of the WiMAX standarad without any error. So the proposed work is designed by NoC based LDPC decode algorithm, which detects and corrects the error (Bayan, A.F., 2010). With this proposed design throughput of the WiMAX, compares with the without LDPC. But the LDPC occupies more area in WiMAX. Synthesis results shows the timing and area constrains and usage of the LDPC. These all explains about the throughput optimization of WiMAX by reducing error-rate from read/write from memory. The main advantage os designing WiMAX using NOC based LDPC is to increase the throughput without any loss of data. But there is possibility of data loss while transmitting the data between the transceiver. Our future work will concentrate about the data loss between the transceiver to increase the throughput of WiMAX transceiver.

Conclusion:

The design of flexible NoC based on LDPC decoder is presented together with the throughput analysis is done for WiMAX. The error status is obtained through the parity bit and the corresponding correction is done by LDPC decoder. The proposed decoder implementation offers a flexibility and full compatibility with the WiMAX standard, which guarantee the highest throughput and low power consumption.

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