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2D Digital Vector Control Algorithm for Cascaded Multilevel Converters

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ABSTRACT

This paper presents a detailed mathematical analysis of 2D vector control algorithm applicable for cascaded multilevel inverters. The algorithm involves evaluation of layer, hex theta, sub sectors, switching vectors and dwell times. Two different topologies of cascaded multilevel inverters are dealt. As the 2D space vectors form a hexagonal pattern with six equal basic sectors, the algorithm is framed for one basic sector and its extension for the other basic sectors highlights the uniqueness of this paper. The analysis is generalized so that it can be applied for any topology and level of inverter. The algorithm is validated by simulation using Matlab/Simulink for both the topologies considered and implementation is done using Nexys 2 Spartan 3E FPGA for hybrid cascaded multilevel inverter.

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INTRODUCTION

Multilevel inverters have been receiving increasing attention in recent decades because of their attractive features such as reduced harmonics producing lower THD, smooth switching and hence less switching power loss etc. The family of multilevel inverters has emerged as a solution for high power applications such as motor drives, High voltage DC transmission, static VAR compensators and static synchronous compensators. The application also extends to medium and low power applications such as electrical vehicle propulsion systems, active power filters, photovoltaic systems and distributed power systems. Recently many researchers have developed different multilevel voltage source inverter topologies (Ilhami Colak, 2010). All these topologies are revision or hybridization of three basic topologies (Rodriguez, J, 2002) Diode clamped (NPC), Flying capacitor (FC) with common DC voltage source for all the cells and cascaded H bridge (CHB) with one DC voltage source for each cell. Among the family of multilevel inverters CHB converters has drawn great interest due to the demand for medium voltage high power applications. More redundant switching states and modularity of CHB offers fault tolerant operation, linear relationship between number of inverter elements and more number of output levels. Output levels can be increased without adding new components instead, by increasing the DC voltages of the supply in geometric progression. Accordingly they are classified as cascaded equal voltage MI (CEMI), Binary Hybrid MI (BHMI), Quasi-linear MI (QLMI) and Trinary hybrid MI (THMI) (Luo &Ye, 2013). The major issue with CHB MLI is that it requires large number of isolated DC sources (L. Maharjan, Franquelo, 2008). Three phase CHB MLI can be realized using various structures. They are,

Type A: Cascading CHB to construct a single phase MLI and connecting three such single phase inverters in phase shifting mode (Rabinovici, R, 2010) as shown in fig. 1.

All the control technique aim to achieve the same goal, to reduce the THD of the current, achieving quality output waveform [T. Ishida, T. Miyamoto, 2002]. The most common and the easiest method is using intersection method (Sub harmonic PWM). The major disadvantage of this method is that it has low output voltage. Space vector approach treats the inverter as a single unit and provides a unique switching pattern based on different switching states. This technique can easily be applied for higher levels and works for all kinds of multilevel inverter topologies. Good utilization of the DC link voltage, low current ripple and relatively easier hardware implementation adds to its advantage [Mekhilef, S.; Kadir, M.N.A, 2011]. Compared to Sub harmonic PWM, space vector approach has 15% higher utilization of the voltage. This feature makes it suitable for high voltage high power applications. The mathematics involved in space vector approach is analyzed in this paper.

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Simulation is performed for type A and type B topologies and experimental verification is made for type B topology. Section 2 describes the circuit operation of type B topology. In Section 3, the detailed mathematical analysis of the 2D digital vector control algorithm is presented. In Section 4, the performance of the algorithm is validated with simulation for both type A and type B topology. Experimental verification was done for type B topology to validate the algorithm is presented in section 5. Section 6 concludes the paper highlighting its major drawbacks.

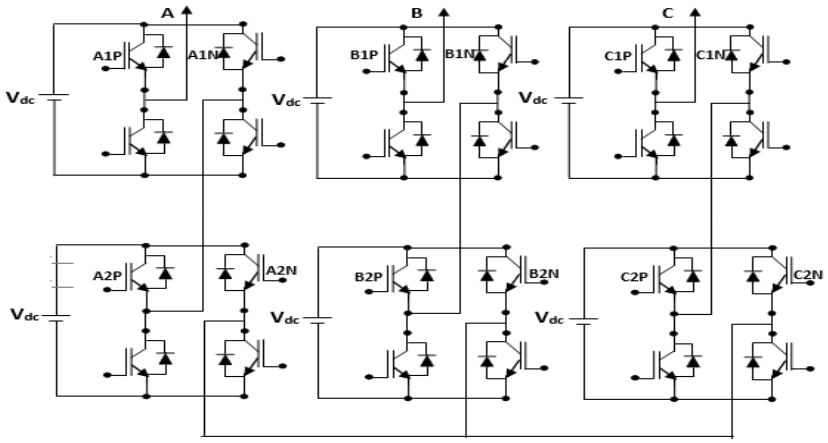

Fig. 1: Type A category of Cascaded Multilevel Inverter.

Type B: Using six pulse inverter as central inverter cell and cascading single phase HB as auxiliary cells with each phase [H. Liu 2008] as shown in fig. 2.

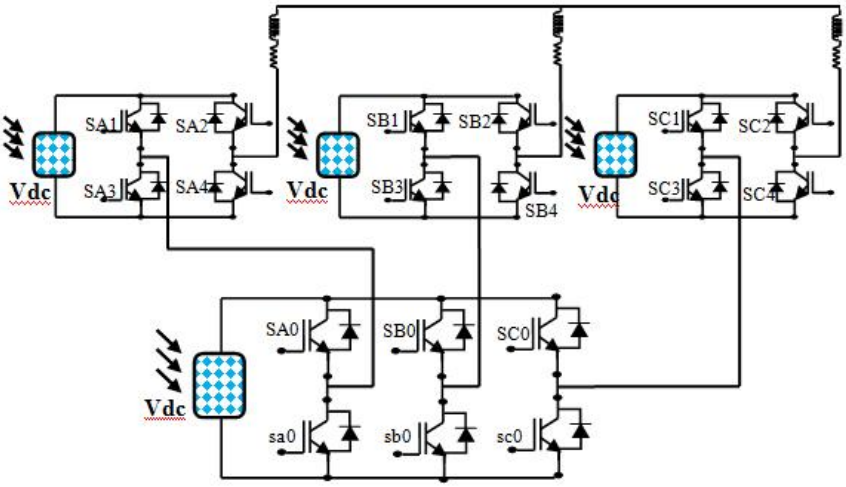

Fig. 2: Type B category of Cascaded Multilevel Inverter.

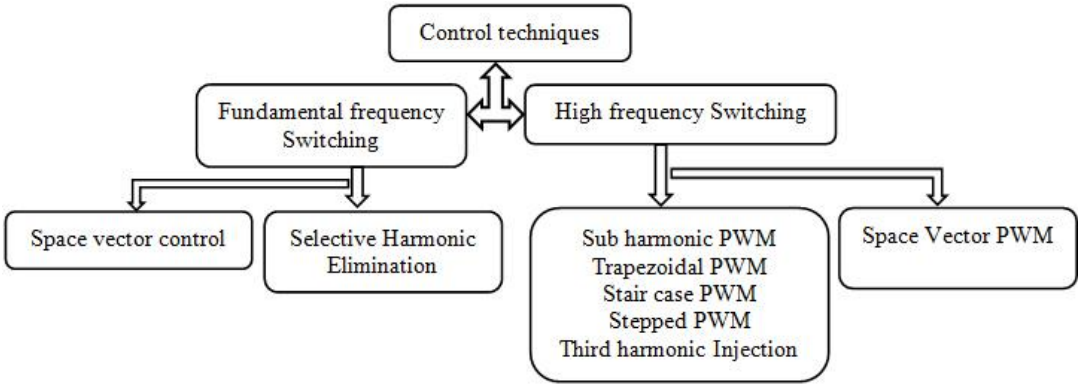

Fig. 3: Classification of Control techniques applied for Multilevel Inverters.

The control strategies for the multilevel inverters as shown in fig. 3. can be classified based on fundamental switching and high switching frequency PWM (Rabinovici, R.; Baimel, 2010).

2. Analysis of Cascaded Multilevel Inverter (CMI):

The type A – 5 level CMI as shown in fig.1 is composed of series H bridge cells. Each cell can provide three voltage levels (+Vdc, 0, -Vdc), the cells are themselves multilevel converters. three such series H bridges are connected in star with the load to form 3 – φ CMI. The configuration of the type B- 4 level CMI considered for analysis is shown in fig. 2. It is composed of a six pulse inverter (main cell) as high voltage cell and a single phase low voltage H Bridge (auxiliary cell) is connected in series with each phase of the central inverter. The main cell and the auxiliary cell are connected to separate DC voltage source (Solar string) of Vdc respectively. The switching states of a branch in the main cell are SA, SB, SC and auxiliary cells are SA1, SB1, and SC1. Each state of the main cell can be assigned with 0 or 1 depending on whether the switches (SA0, SB0,SC0) connected to positive terminal of the DC source is OFF or ON as in Table 1a and that of auxiliary cell can be -1, 0 or 1 and described in Table 1b. Among the 2S (where S is number of switches) available switching states only 2b (where b is number of branches) states are valid satisfying the following conditions: The sources must not be short circuited and The load must not be left open. More number of levels in output vo1tage can be achieved by connecting additional H bridges in series for both the topologies.

Table 1: Switching States corresponding to Inverter switch Conduction.

Switch SO	State
ON	1
OFF	0

(a) Main Cell

Switch S1		State
Sa1	Sa2	
OFF	OFF	0
OFF	ON	1
ON	OFF	-1
ON	ON	0

(b) Auxiliary Cell

3. Mathematical Analysis of Clarke transformation Approach:

The algorithm is framed considering type A topology as it contains more number of layers. It is also generalized so that it can be applied for any topology of cascaded multilevel inverter. The algorithm is developed assuming that the DC sources are equal.

Generation of space vectors:

For type A and B 3- φ topology, considering all the DC sources from the solar strings are equal the total number of switching states (Ns), Active vectors (Nav) and redundant vectors (Nre)

Table 2: Analysis of vectors.

	Type A	Type B
Ns	125	189
Nav	61	37
Nre	64	152

When the DC sources vary due to array reconfiguration or shading effect the redundant vector reduces and hence the active vectors increases. The three dimensional (Vabc) plane containing three phase voltage are transformed to a two dimensional plane (α, β) using Clarke's transformation. The space vectors corresponding to any state of MLI can be obtained using Eqn. 1.

$$V_s = V_{an} + V_{bn}.e^{j2\pi/3} + V_{cn}.e^{j4\pi/3} \quad (1)$$

$$\propto = V_a + V_b * \cos\frac{2\pi}{3} + V_c * \cos\frac{4\pi}{3} \quad (2)$$

$$\beta = V_b * \sin\frac{2\pi}{3} + V_c * \sin\frac{4\pi}{3} \quad (3)$$

Plotting α vs. β generates the space vector pattern as shown in fig. 4a &4b.

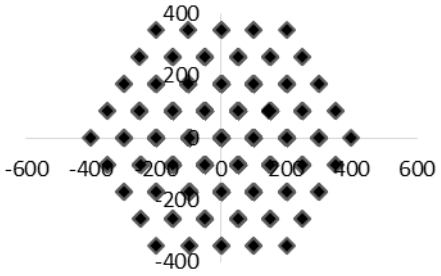

Fig. 4a: Vector pattern for type A topology.

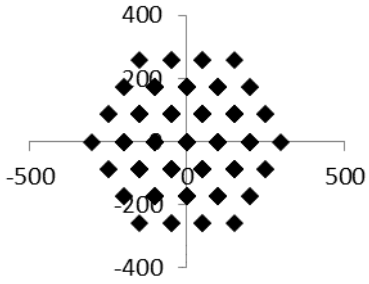

Fig. 4b: Vector pattern for type B topology.

From the vector pattern, it is evident that the space vector form a hexagonal pattern. The number of hexagons depend on the level (N) of the inverter. The number of hexagons for type A and B topology are 4 and 3. As the hexagon can be divided equally into 6 basic sectors (BS) displaced by 60˚ as shown in fig. (5a). The algorithm is framed for one BS which can be extended to other basic sectors.

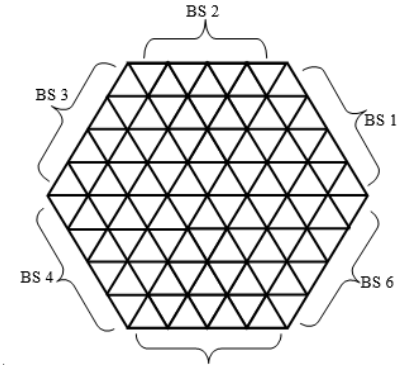

Fig. 5a: Six Basic Sectors.

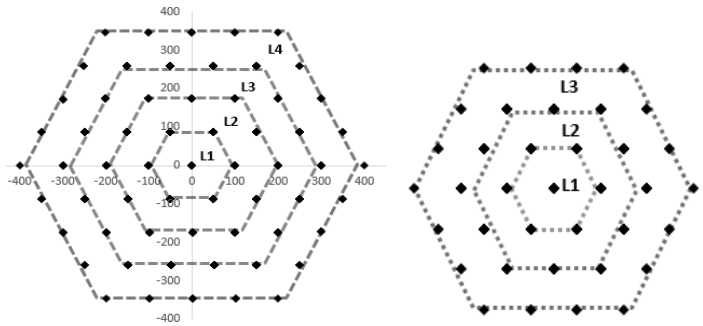

Fig. 5b: Number of layer for Type A and Type B topology.

Determination of magnitude $|A|$, theta θ and Layer (L):

Having found α and β magnitude and theta can be calculated as $|\mathbf{A}| = \sqrt{\alpha^2 + \beta^2}$, $\theta = \tan^{-1}\beta/\alpha$. Layer (L) is defined as the space enclosed by the vectors between hexagons. The number of layers is equal to the number of hexagons formed as shown in fig. 5b for both the topology. Based on the theta and magnitude of the instantaneous reference vector, layer is identified. From the vector distribution it can be observed that for a particular DC voltage and modulation index the maximum obtainable voltage is 400 and 300 for type A and B topology respectively as shown in fig. 5b. Considering type A topology and BS 1, α and β are normalized to simplify the computation. As the maximum output voltage is 400, it is normalized to (4↔M) as shown in fig. 6. Upon normalizing, the width of the hexagon from the origin can be determined as (1/M, 2/M, 3/M and 4/M), where L= 1, 2, 3, 4

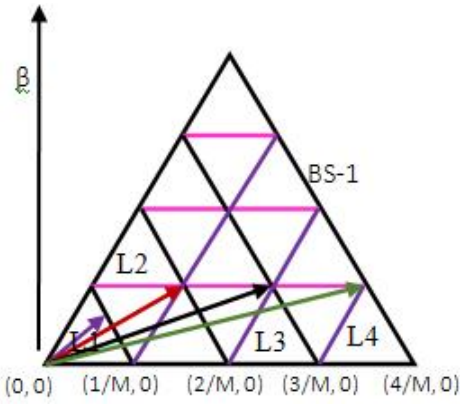

Fig. 6: Normalizing the output voltage to simplify computation.

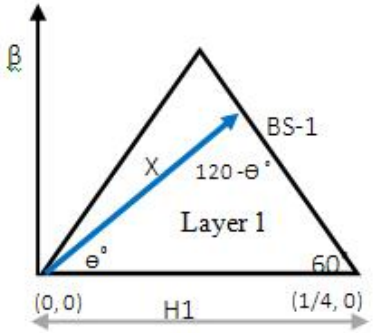

Fig. 7: Layer and Basic sector 1.

Considering layer and BS 1 as shown in fig. 7. Applying law of sine to solve oblique triangles, the width of the

H1 from origin can be found or the maximum magnitude of the rotating reference space vector (X → Vref) to lie in layer 1 with respect to the ɵ˚ can be found using the expression.

$$\frac{\mathbf{X}}{\sin(60°)} = \frac{1/4}{\sin(120°-\theta°)} \quad \Longmapsto \quad \mathbf{X} = \frac{\frac{1}{4}*\sin(60°)}{\sin(120°-\theta°)} \tag{4}$$

The above expression for X (magnitude) can be generalized for any layer by replacing 1/4 as [(L/M)] where L = 1,2,3,4 …. Having found the maximum magnitude for each layer, layer in which the instantaneous space vector lies can be easily obtained.

Determination of Hex theta (HT) and Sector Identification:

The angular displacement between the adjacent vectors in the succeeding layer decrease is referred as hex theta. It can be determined as.

HT = 60˚/ Corresponding L (5)

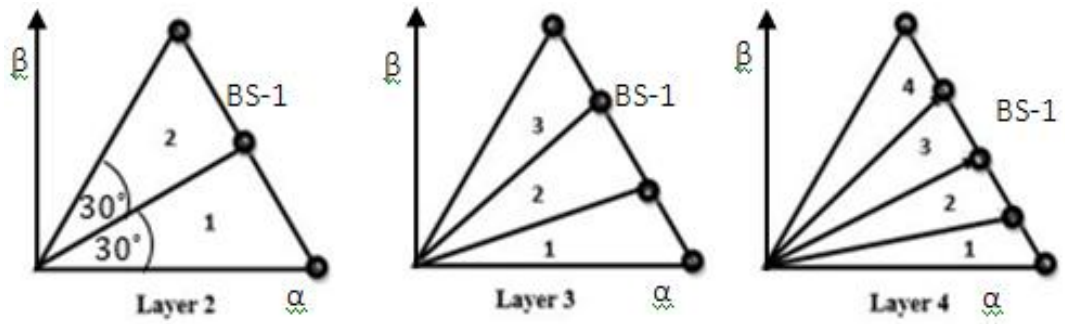

Fig. 8: Decrease in Hex theta with increase in layer.

Considering Layer 2, Hex theta = 30˚, hence the BS is divided into 2 sectors in L2 with its angle varying between 0 ˚ to 30˚ in each sub sectors. BS are further divided into sub sectors (SS) in each layer. The number of SS increases with increase in L and decrease in HT. as shown in fig. 8 and Tab. 3

Total No of sub sectors in each layer = (60˚/ L) * L (6)

Table 3: Relation between hex theta, layer and sub sector.

Hexagon/ Layer	Hex theta	Sub Sector In each layer
1	60˚	6
2	30˚	12
3	20˚	18
4	15˚	24

Based on the steps 1 and 2 the number of sectors for each layer can be generalized as

$$[0\ to\ (L-K)*HT]*1 \quad for\ L1 \tag{7}$$
$$[(L-K)*HT\ \ to\ (L-(K-1))*HT]*2 \quad for\ L2 \tag{8}$$
$$[(L-(K-1))*HT\ \ to\ (L-(K-2))*HT]*3 \quad for\ L3 \tag{9}$$
$$[(L-(K-2))*HT\ \ to\ (L-(K-3))*HT]*4 \quad for\ L4 \tag{10}$$
$$[(L-(K-n))*HT\ \ to\ (L-(K-n+1))*HT]*L \quad for\ Ln \tag{11}$$

Where L = 1, 2. . . N-1, n = 0, 1, 2. . K, K = (L-1) and HT = Hex theta.

Identification of triangle:

At any instant of time the reference vector is enclosed by three vectors which forms a triangle. Due to uniform distribution of the space vectors the triangles so formed are equilateral triangles. The number of triangles increases with layers as shown in fig. 9

Total No of Triangles in each layer = $L+(L-1)]$ (12)

Fig. 9: Number of triangles.

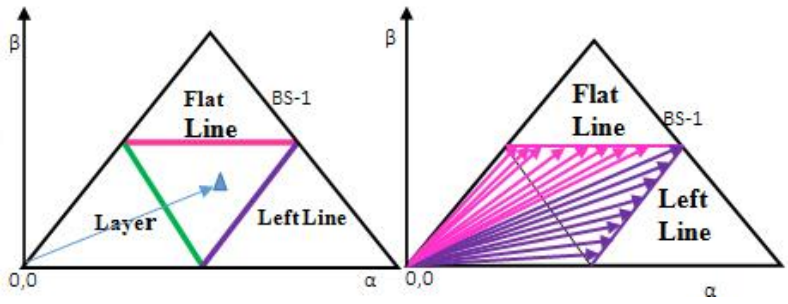

Fig. 10: Three lines of a triangle.

To exactly identify which triangle enclose the rotating reference vector the equation of the three lines as shown in fig. 10 flat line - FL, left line - LF and the layer- L has to be determined with respect to theta. Using simple geometry, it can be stated that when the rotating reference vector traverse on the line, it represents the equation of the line itself with respect its angular displacement. By applying law of sine to triangle (ABC) shown in fig. 11, the equation of the left line can be generalized. It is (L-1) because it lies between layers.

$$x = \frac{(L-1)/4}{\sin(60° - \theta°)} * \frac{sin(120°)}{1} \tag{13}$$

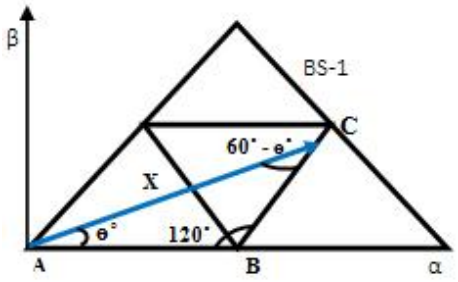

Fig. 11: Triangle ABC – Left Line equation.

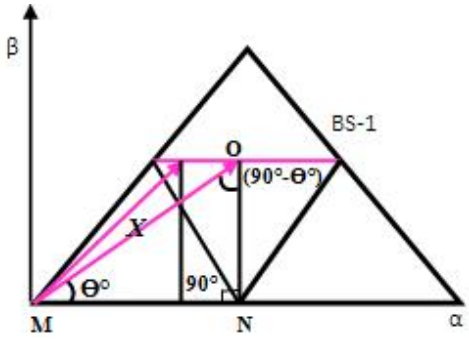

Fig. 12: Triangle MNO – Flat Line equation.

Since all the triangles are equilateral triangles, the height of the triangle as shown in fig.13 is √3/2. Therefore equation of the flat line as shown in fig.12 is can be generalized considering the triangle MNO.

$$x = \frac{\frac{\sqrt{3}}{2} * L/4}{\sin(\theta°)} * \sin(90°) \tag{14}$$

The coordinates of the triangles can be found using simple geometry as shown in fig. 13 Having known the three equations of the line and the coordinates of the triangles it is possible to find exactly where the rotating reference vectors lies and hence use the vertices of the triangles to calculate the duty cycle.

Selection of Vectors:

Appropriate vectors (V1, V2 and V3) and its corresponding layer has to be selected in order to minimize the harmonic distortion and number of switching per sample period. For selection of V1 and V2 only the first

BS is selected, and how it can be extended to the other sectors is also dealt. The fig.14a, indicates the numbers assigned to each triangle which are then normalized to enhance easy computation as shown in fig.14b. The normalized triangles are further scaled down to 1 and 0 fig.14c, where 1 denotes odd numbered triangles and 0 denotes even numbered triangles. In other words 1 denotes normal triangle and 0 denotes inverter triangle as in fig.14d, fig. 14e since it is required to select the correct sequence in which V1, V2 and V3 have to be selected.

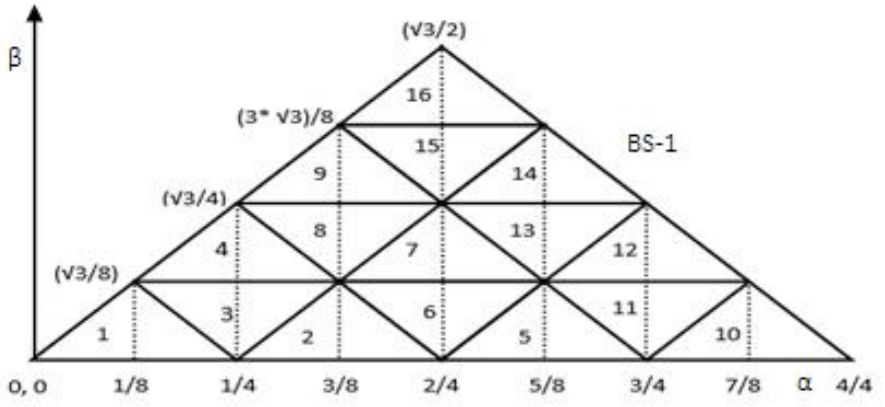

Fig. 13: Coordinates of the triangles.

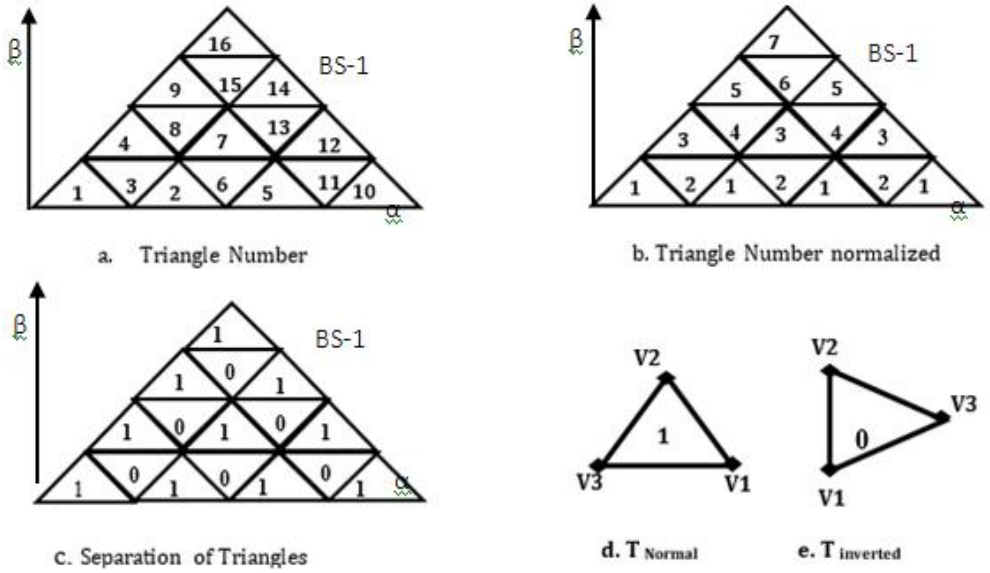

Fig. 4: Selection of vectors.

Considering that the reference space vector traverse through the L2, the appropriate nearest vectors that has to be selected is depicted in fig (15 a-d). Generalizing for all BS, mathematically it can be formulated as

For normal or odd numbered triangle,

$$V1 = \frac{T_{NM}}{2} + [(BS-1) * L] \quad (15)$$

$$V3 = V1 - [(BS-1)] \quad (16)$$

For inverted or even numbered triangle,

$$V1 = T_{NM} - int\left(\frac{T_{NM}}{2}\right) + [(BS-1) * (L-1)] \quad (17)$$

$$V3 = V1 + BS \quad (18)$$

For both odd and even numbered triangle

$$V2 = (V1 + 1) \quad (19)$$

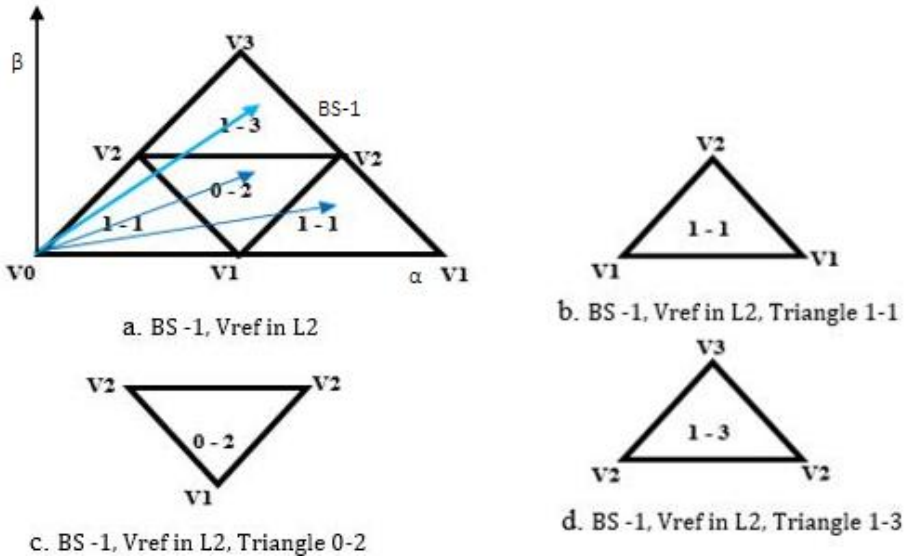

Fig. 15: Sequence of vector selection.

Having found the nearest three vectors, it is to be noted from the fig. 15 that V1, V2 and V3 are selected from different layers of the hexagon. Hence it is required to find V1, V2 and V3 of which layer has to be selected.

For normal or odd numbered triangle,

Layer for V1 and V2 = L, Layer for V3 = (L – 1) (20)

For inverted or even numbered triangle,

Layer of V1 and V2 = (L – 1), Layer for V3 = L (21)

Determination of dwell time and duty cycle:

The ON time of the switches depend on the duty cycle of three switching vectors. From Fig. 16 by vector addition to synthesize reference voltage (V_r), Equation (22) must be satisfied. Solving Equations (23), (24) and (25) D1, D2 and D3 can be determined.

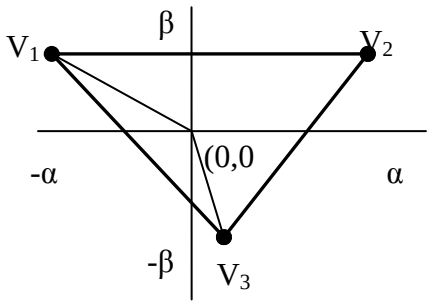

Fig. 16: Reference vector Synthesis..

D1*V1 +D2*V2+D3*V3 = Vr (22)

This implies that

D1*X1 +D2*X2+D3*X3 = 0 (23)

D1*Y1 +D2*Y2+D3*Y3 = 0 (24)

Where Di is duty cycle and Xi, Yi are co-ordinates of Vi with reference to Vr (where i = 1, 2, 3) and since V1, V2 and V3 encloses Vr.

D1 +D2 +D3 =1 (25)

Equation (23) and (24) suggests a way to use PWM to generate a three phase voltage of which the average value follows a given three phase reference by switching among the vectors V1, V2 and V3 with duty cycles D1, D2 and D3 respectively.

4. Simulation Results:

The performance of the proposed modulation technique has been validated for both the topologies using Matlab / Simulink as shown in fig. 17 with R–L load. The simulation parameters are shown in Table. 4

Table 4: Simulation Parameters.

Quantity	Value
R-L Load	R = 20Ω, L =27 mH
Main cell and Auxiliary cell voltages (Vdc)	100 V (fixed)
Output Voltage frequency	50 Hz
Switching frequency	5 kHz

The steps involved in simulating the digital control algorithm to generate the switching pattern are

1. Generation of space vectors
2. Determination of magnitude, theta and layer
3. Determination of hex theta and sectors
4. Determination of triangle and its co-ordinates
5. Selection of vectors

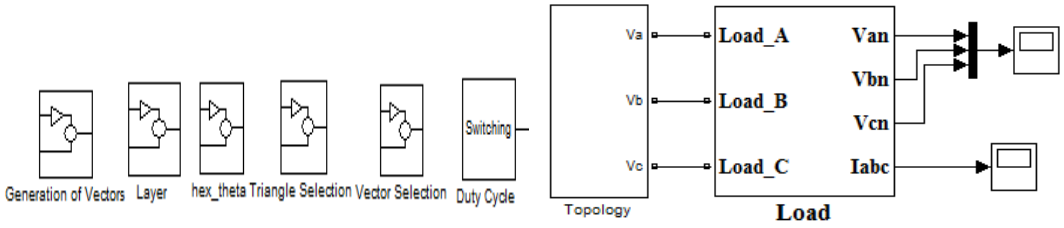

Fig. 17: Matlab/Simulink simulation blocks.

Calculation of dwell time, duty cycle and hence switching pulses

The load voltage and load current waveforms obtained for Type A topology is shown in fig. 18.

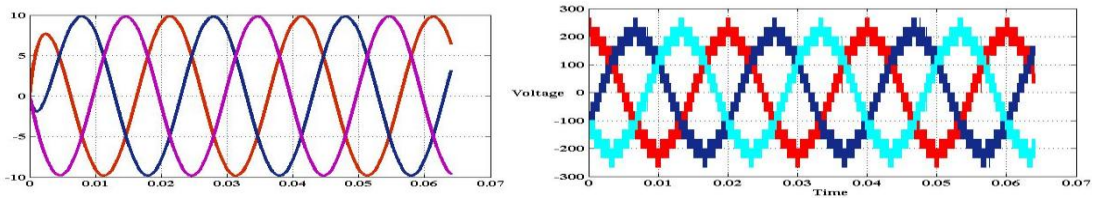

Fig. 18: Load Voltage and Load current waveforms of Type A topology

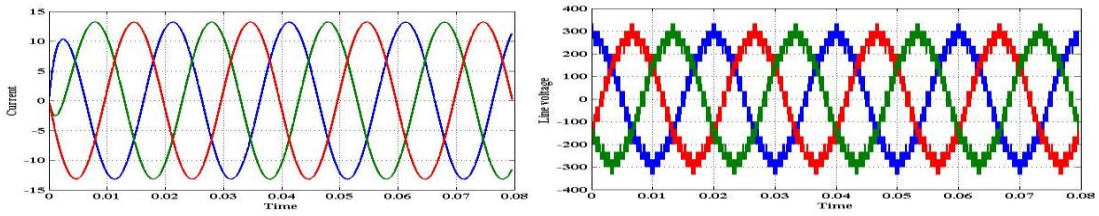

Fig. 19: Load Voltage and Load current waveforms of Type B topology.

The Phase voltage and load current waveforms obtained for Type B topology is shown in fig. 19.

5. Hardware Results:

The Cascaded Multilevel Inverter of type B was built using four smart power IGBT (FSBB20CH60B) modules as shown in Fig 20 with built in gate driver. The modules are fixed with suitable heat sink and snubber circuit for protection. A diode rectifier is provided at the input for AC to DC conversion. Hall sensors are provided for current measurement. The developed algorithm was implemented using Nexys 2 Spartan 3E – FPGA. Agilent oscilloscope has been used to capture the waveforms. For load a 3-ϕ star connected Induction motor of 0.5 Hp rating was considered. The Dc supply for the module were fed from solar panels as in fig. 20a.

The details of the panel details are shown in Table 5. Due to practical difficulties the wiring from the panels was brought down and experiment was conducted. The results obtained are shown in fig. 21a and fig. 21b.

Table 5: Details of Solar panel – Make Bharat Electronics.

75Wp	Irr = 100mw/cm2	Temp = 26°C	Voc = 21.98V	Isc = 5.258A	Vmp = 17.48	Imp=4.77

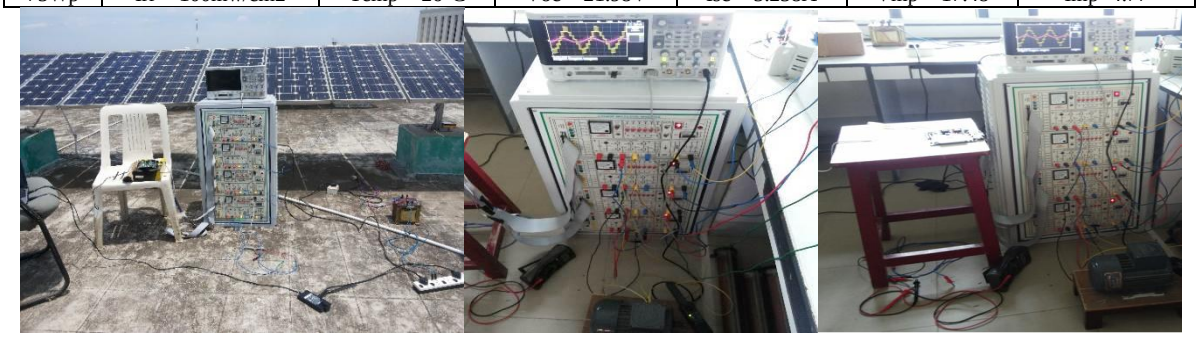

Fig. 20a: Experimental Set up fed from Solar Panels.

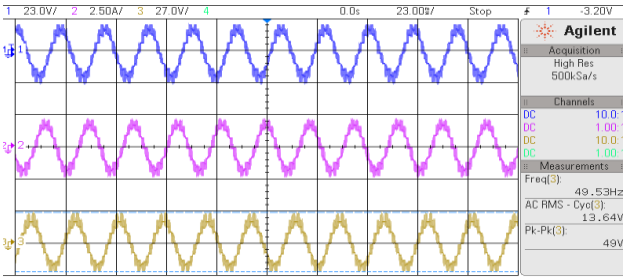

Fig. 21a: Load Voltages of three phases.

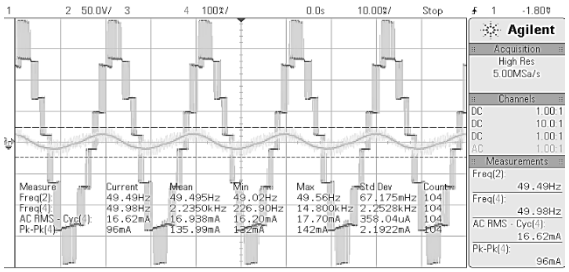

Fig. 21b: Load voltage and current obtained.

Conclusion:

In this work a 2D digital control algorithm is framed for cascaded multilevel inverters with equal voltage source. Although new control algorithm is proposed in the literature, the fundamentals has to be understood. The mathematics involved in framing the algorithm is explained in detail. The developed control is validated by simulating for two different cascaded multilevel inverter topologies and implemented for a hybrid cascaded inverter topology. The simulation and experimental results proves that it can be employed to any type and level of cascaded inverter topology. The major drawback of this method is that it cannot be applied for abnormal or uneven distribution of vectors or for unequal DC voltages.

REFERENCES

Amit Kumar Gupta, M. Ashwin Khambadkone, 2006. A Space Vector PWM Scheme for Multilevel Inverter Based on Two-level Space Vector PWM. IEEE Transactyion on Industrial Electronics, 53(5).

Franquelo, L.G., J. Rodriguez, J.I. Leon, S. Kouro, R. Portillo, M.A.M. Prats, 2008. The age of multilevel converters arrives. Industrial Electronics Magazine, IEEE, 2(2): 28-39.

Ilhami Colak, Ersan Kabalci, Ramzan Bayindir, 2010. Review of Multilevel voltage source inverter topologies and control schemes. Journal of Energy Conservation and Management.

Ishida, T., T. Miyamoto, T. Oota, K. Matsuse, K. Sasagawa and L. Huang, 2002. A control strategy for a

five-level double converter with adjustable dc link voltage. Industry Applications Conference, 1: 530–536.

Laxminarayanana, G., K. Pradeep, 2013. Comparative Analysis of 3, 5 and 7 level inverter using space vector PWM. International journal of advanced Research in Electrical, Electronics and Instrumentation Engineering.

Liu, H., L.M. Tolbert, S. Khomfoi, B. Ozpineci and Z. Du, 2008. Hybrid cascaded multilevel inverter with PWM control method. Proc. IEEE 39th Power Electron. Spec. Conf., Rhodes, Greece, pp: 162–166.

Maharjan, L., S. Inoue and H. Akagi, 2008. A transformerless energy storage system based on a cascade multilevel PWM converter with star configuration., IEEE Trans. Ind. Appl., 44(5): 1621–1630.

Mekhilef, S., M.N.A. Kadir, 2011. Novel Vector Control Method for Three-Stage Hybrid Cascaded Multilevel Inverter. IEEE Transactions on Industrial Electronics, 58(4): 1339-1349.

Rabinovici, R., D. Baimel, J. Tomasik, A. Zuckerberger, 2010. Series space vector modulation for multi-level cascaded H-bridge inverters. Power Electronics, IET, 3(6): 843-857.

Rodriguez, J., Jih-Sheng Lai, Fang Zheng Peng, 2002. Multilevel inverters: a survey of topologies, controls, and applications. IEEE Transactions on Industrial Electronics, 49(4): 724-738.

Wei, S., B. Wu, F. Li and C. Liu, 2003. A general space vector PWM control algorithm for multilevel inverters. Applied Power Electronics Conference and Exposition, Eighteenth Annual IEEE, 1: 562–568.