AENSI Journals

Australian Journal of Basic and Applied Sciences

ISSN:1991-8178

Journal home page: www.ajbasweb.com

Design of Novel Routing Switches for Power Optimization in FPGA Routing Circuits

[1]Sundar Prakash Balaji M. and [2] Vijayan S.

[1]*Assistant Professor, Department of ECE, RVS Faculty of Engineering,Coimbatore, India*
[2] *Prncipal, Surya Engineering College, Erode, India*

ARTICLE INFO

Article history:
Received 19 August 2014
Received in revised form
19 September 2014
Accepted 29 November 2014
Available online 15 December 2014

Keywords:
FPGA,Power,PDP,Dynamic power.

ABSTRACT

At present scenario, power consumption in the leakage mode is much lower than the sleep mode .It is suitable for the routing switches that are not used in the FPGA routing circuitry. The new switches are inspired through an analysis FPGA design. We proposed a technique which introduces low-power solution using a single circuitry to control the voltage in active, sleep and drowsy voltage control mode. In active mode, voltage scaling is implemented for reducing the power dissipation. In sleep mode, intermediate power saving, leakage current is reduced and prevents the data withholding. In Drowsy mode, power is prevented in gating structure of the circuit. The proposed system operates on two types of voltage control mode, in which transistor count and FPGA routing are reduced. In mode I: voltage scaling is analyzed in active, drowsy and sleep mode. In mode II: voltage scaling is analyzed in active and sleep mode. While comparing the various modes of operation, power delay product (PDP), energy efficiency and dynamic power are reduced. In mode I operation, power reduction of 4.5% is achieved and in mode II operation power reduction of 5% is achieved compared to the existing FPGA routing system.

To Cite This Article: Sundar Prakash Balaji M. and Vijayan S.., Design of Novel Routing Switches for Power Optimization in FPGA Routing Circuits. ***Aust. J. Basic & Appl. Sci.,*** *8(18): 490-495 2014*

INTRODUCTION

The optimization of placement problem in FPGA has to be done through assigned positions among the interconnecting cells. In each layer, the area overhead and the interconnect is analyzed using net list. Routing is normally performed in two stages; global routing which determines the wiring channels and how the interconnection is done and the précis path is processed through local routing or detailed routing. The area routing problems are processed through various algorithms such as path connection or maze routing algorithm. By making use of source and target ,the basic routing algorithm is processed.

There are many routing problems, which are analyzed based on the number of wiring layers and how the orientation of wire segments in a given layer use their segment structure. In grid routing, the spacing between the lines are analyzed (Betz and Rose, 1999). The number of available wiring layers depends on the technology and the design style. Recent developments have led to technologies that make several more layers available. At present scenario, FPGA routing will be an active research topic. It is due to the evolution of enormous utilization of logical blocks and routing resources.

In FPGA, the supply voltage of the look-up table is dual V_{dd}, whereas we propose a system which uses single V_{dd}. Fig.1 shows a routing switch which is the combination of MUX tree and SRAM cells. Memories in the LUT can be programmed to put into practice for four-input logic function which helps to reduce the dynamic power with respect to the supply voltage (Fei Li et al. 2004).

Technical back ground:

In the designed circuits, routing is an important step in FPGA architecture which is completely based on how the interconnection is done and those interconnection delays dominates the logic delays. The proposed structure outperforms the existing performance of the circuit based on total length of the critical path which includes wiring. In classical models, all the wires run along orthogonal grid lines with uniform separation .The routing problem minimization is made use of switch box to find out the existing possible solution .Three different modes of operation in FPGA design helps to overcome the drawback of the existing method which in turn helps to lower the FPGA routing power consumption. Finite wire length is an important aspect in routing

Corresponding Author: Sundar Prakash Balaji M., 1Assistant Professor, Department of ECE, RVS Faculty of Engineering,Coimbatore, India

which helps to reduce the path delay in lower power routing switches. It should be of tri-state or pass transistor and besides it is configured with proper width and spacing. Power consumption is reduced in low-power mode due to optimization in Power-delay product (PDP) which switches the routing switches and operated on different modes. Fig. 1 shows a traditional FPGA routing switch (Safeen Huda et al. 2009) .

The programmability for different applications are based on large number of transistors used in the circuit construction, at present scenario power reduction in FPGA pays more attention. In this paper, a hierarchical interconnect architecture is introduced by making use of low-swing long wires which helps to reduce power dissipation. In turn, predefined dual V_{dd} and dual V_t has provided the possibilities to reduce dynamic power which plays a major role in power optimization. The increase in the supply voltage leads to higher performance of the circuit, but in turn increases power consumption. Through V_{dd} scaling, we will be able to lower the supply voltage which is passed to the entire design to reduce power. Alternatively, dual-V_{dd} provides high supply voltage (V_{ddH}) on critical paths and low supply voltages (V_{ddL}) for non critical paths (Fei Li et al.2004).

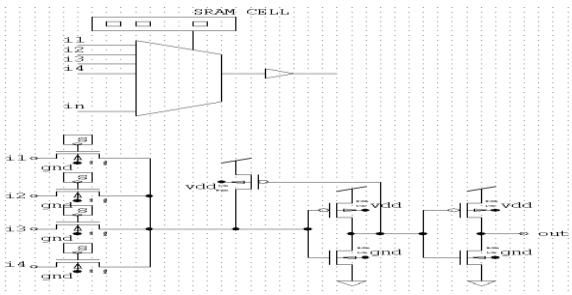

Fig. 1: Low power routing switch.

Fig.1 illustrates the transistor-level view of low power routing switch. It consists of multiplexer, a buffer and SRAM configuration cells. In FPGAs the construction of multiplexers are done through NMOS transistor tree. The inputs are tolerated to weak-1 signals. The level-restoration in FPGA routing switches is tolerable only if logic-1 input signals need not to be railed. The main exception to this observation are switches that drive inputs on logic blocks. The proposed new switch design is based on the observations, how those switches which drives input signals to the logical blocks. The switch includes n-MOS and p-MOS sleep transistors in parallel. Power in the gating structure which is operated in different operating modes is designed through the parallel clamped PMOS with NMOS tree structure (Alioto and Palumbo, 2005). Voltage gap of MOS transistors are reduced when they are connected in parallel. (Y.Ji-renet, 1989) proposed multiple power modes for the circuit , but it needs multiple supply voltages which aids in operating at different threshold voltages, but it is costly option. (Pelleranoet,2004) and (Luca Cicarelli et al. 2004) implemented a negative feedback technique with a sleep inverter, but it fails since leakage power consumption is more in the system. In this section, we propose a circuit which consist of P-MOS and N-MOS switches. We propose a system which optimizes power using a single routing switch. It operates on three modes Active, sleep and drowsy.

Low-Power Switch Design:

In the designed routing switch which inputs to weak signals ie, logic-1 input signals and it is acceptable only if it is lower than the logic-1 input signal. The time slack problem in the overall FPGA routing switches is lowered through special handling routing techniques. The inputs that drive to the logical blocks are observed based on the proposed switching architecture specified on the design as shown in Fig. 3(Anderson and Najm, 2009) in which the pull up and pull down transistors are arranged parallel to each other. The switch works in various modes of operation as follows: Those operations are used to reduce the threshold voltage, switching energy and current leakage occurring in transistors in different modes of operation. In order to reduce excessive current leakage in the circuit design, multiple high supply voltages at chip level is proposed in (Anderson and Najm, 2004). In order to avoid excessive leakage in circuitry, this is operated at high supply voltages and processed through level converters. In each routing switch of additional configuration SRAM cell is realized through the selection of various operating modes (Navid Azizi and Farid Najm, 2004).

The proposed system outperforms the traditional approach in terms of post-routing complexity in FPGA design where time slacks are already known by the routing stage.

Circuit Configuration:

The circuit consists of SRAM, multiplexer and MTCMOS logic. The transistor switch consists of P-MOS and N-MOS transistors. For unused routing switches, the power consumption in leakage mode is much lower than the sleep mode (Mingjie Lin and Abbas El Gamal, 2008). In CMOS, static power dissipation in SRAM-

based FPGAs occurs mainly due to current leakage. 1) Reverse biased current in p-n junction 2) Sub threshold channel conduction are the two major sources of leakage current. In cooperation, these parameters have comparable uniqueness such as process variation, logic states of the circuit and high dependency to temperature. Whenever, the transistors are scaled, a leakage current is unnoticed due to insignificant amount but it is expected to change whenever the transistor dimensions are scaled down. (Li Shang and Alireza Kaviani, 2004).

In Low Power: 1. Power consumption is reduced through optimized speed and 2. Reduction in the leakage is due to output swing by V_{th}. 3.Depending upon the routing switch, dynamic power is reduced low power mode. In Sleep Mode: 1. Leakage power occurs which in turn, is nominal when compared to high speed mode. 2. The proposed design outperforms the traditional routing switch which involves relatively small area.

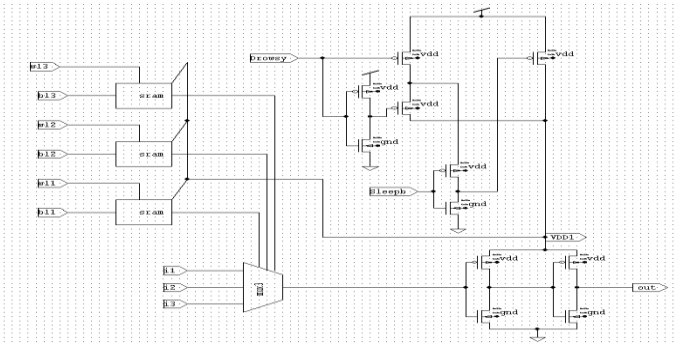

Fig. 2: Routing switch for Mode-I Operation.

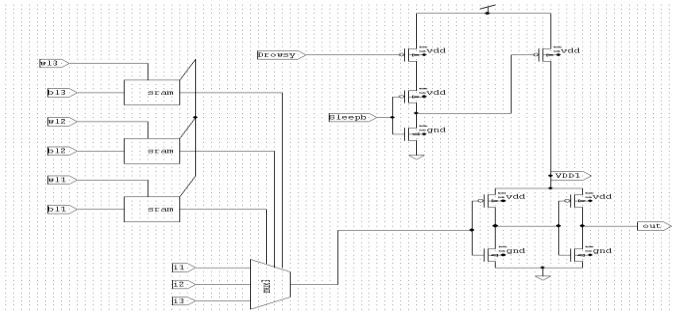

Fig. 3: Mode-II Operation.

Table I: Mode-I Operation.

	Mode-I	
Sleep	Drowsy	Function
1	X	Active
0	0	Sleep
0	1	Drowsy

a.Mode- I:

The three distinct modes of operation are illustrated in Table I. The data retention in the power gating design is implemented through the proposed tri-modal switch which has the ability to retain data in the drowsy mode. The proposed tri-modal switch is designed based on distinct low power design methodologies such as data-retentive power gating, multi-drowsy mode structure and on-chip dynamic voltage scaling.

b.Mode-II:

This mode which outperforms in all distinct three modes of operation such as sleep, active and drowsy than the existing mode of operation. When sleep enabled EN=1, tri state circuit operates depending on level of input pulses. If drowsy EN=1 negative feedback pulses generates which block the circuit from grounding. When sleep or drowsy EN=0 circuit is in active mode. But under a condition as Sleep = 0 and drowsy is high, and then circuit becomes drowsy. At this condition power leakage is high. To overcome the power losses in the circuit, transistors are included to reduce losses. The typical circuit is as shown in Fig. 3 and Table-I.

Simulation analysis:

The proposed routing switch is analyzed based on the previously designed traditional routing switch methodology in which the rise and fall times of the buffer are equal. The output response with respect to input

parameters of the multiplexer is analyzed and the power characteristics of the proposed switch are simulated in cut off, linear and nonlinear regions. Power and the various performance measurements are tabulated as shown in Table III. The current drawn from various sources such as the multiplexer, SRAM configuration cells and sleep transistors consumes power and the corresponding values are tabulated as shown in Table III. The tabulated results show the proposed routing switch offers large leakage current reduction which is operated at high speed than the traditional switch design.

Table II: Mode-II Operation.

Mode-II		
Sleep	Drowsy	Function
1	X	Active
0	0	Sleep

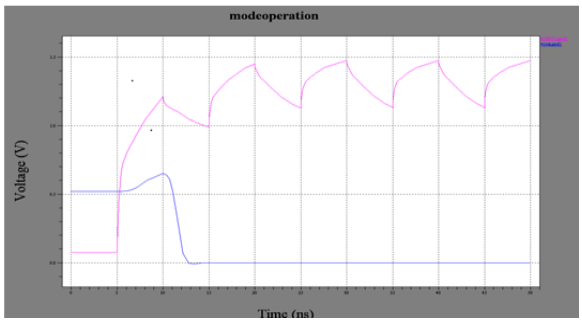

Fig. 4: Simulation results for Mode Operation – I.

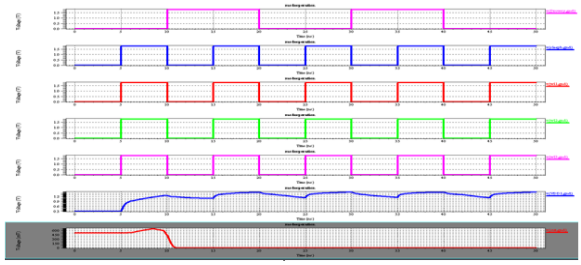

Fig. 5: Simulation results for Mode Operation – II.

Table III: Summary of results for existing and proposed routing switch designs.

Parameter	FPGA Routing	Mode operation I	Mode operation II
Power	4.944988e-002	2.276691e-003	1.3109e-003
Static power	1.9246e-004	2.099e-004	2.0101e-004
PDP	8.6607 e-012	11.271 e-013	10.66e-013
EDP	38.961 e-020	59.85 e-22	46.46e-022
Static current	0.106uA	0.1166uA	0.1116uA

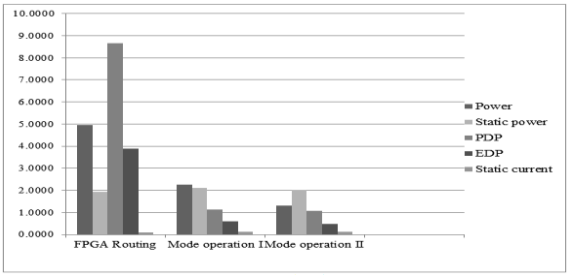

Fig. 6: Power analysis of existing and proposed routing switches.

The power consumed by the existing dual V_{ddL} is given by 4.944988e-002, and its static power is 1.924651e-004 and its dynamic power is 3.411741e-004. The power consumed by mode-I operation is 2.27669e-003 watts, and its static power is 2.09924e-004 and its dynamic power is 2.179506e-010. The power consumed by proposed mode-II operation is 1.31099e-3 and its static power is 2.0101e-004 and its dynamic

power is 1.2143e-10 .The simulation results infer that the power dissipation in FPGA is reduced in the proposed mode-I and mode-II operations (Shang Kaviani and Bhathala, 2002) compared to the existing FPGA routing system. The parameters of the FPGA routing circuitry is illustrated in (Sundar Prakash Balaji and Vijayan, 2012).

In Fig.7.the design has the same statistical behavior. This is sensitive because these resources are driving each other and routing resources may change the switching activity. It helps to reduce the power dissipation. Fig.8. illustrates that the leakage current is reduced with respect to standby mode in data holding. Fig.9. illustrates that the transient delay is reduced due to the energy efficiency and it has increased in mode II operation compared to other modes.

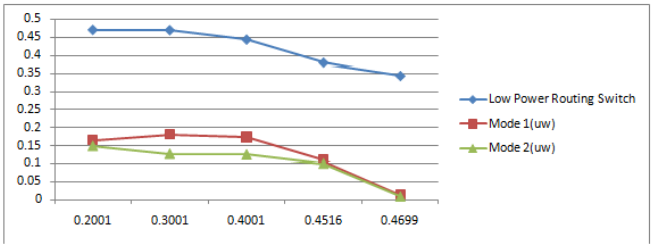

Fig. 7: Power (uW) comparison results of existing and proposed (Mode I and II) routing switches with time scale.

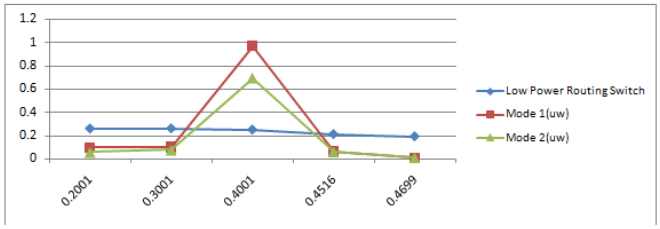

Fig. 8: Current (uA) comparison results of existing and proposed (Mode I and II) routing switches with time scale.

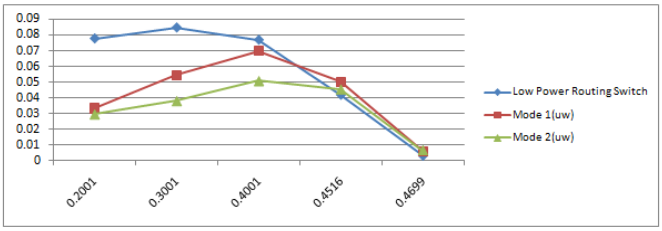

Fig. 9: PDP (Pw/s) comparison results of existing and proposed (Mode I and II) routing switches with time scale.

Conclusion:

In this paper, we have proposed two new routing switch designs which are programmed to operate in high power, low power and sleep mode. Each of the proposed switch offers different power/PDP/EDP/ Static current. Table III illustrates the power comparison results of existing and proposed routing switches. The results show that 5% of the power reduction is achieved. Power results are analyzed using TANNER tool .The technology used is 0.18um and its supply voltage is 1.8v to 2v.

ACKNOWLEDGEMENT

The author would like to thank his research Supervisor Dr.Vijayan Subramanian for his consistent encouragement and support in carrying out the research work.

Australian Journal of Basic and Applied Sciences, 8(18) December 2014, Pages: 490-495

REFERENCES

Betz, J., Rose, 1999. FPGA Routing Architecture: Segmentation and Buffering to Optimize Speed and Density. In the Proceedings of the ACM/SIGDA seventh international symposium on field programmable gate array, 59-68.

Fei Li, Yan Lin, Lei He i, 2004. FPGA Power Reduction Using Configurable Dual-Vdd. In the Proceedings of the 2004 Annual Conference in Design Automation, San Diego, California, USA, 735-740 .

Safeen Huda, Muntasir Mallick, Jason H. Anderson, 2009. Clock gating architectures for FPGA power reduction. IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, 112-118.

Fei Li, Yan Lin, Lei He and Jason Cong, 2004. Low-Power FPGA Using Pre-defined Dual-Vdd/Dual-Vt fabrics. In the Proceedings of the ACM/SIGDA 12th International Symposium on Field Programmable Gate Arrays, Monterey, California, USA, 42-50.

Alioto, M. and G. Palumbo, 2005. Model and Design of Bipolar and MOS Current-Mode Logic Digital Circuits. Springer, New York.

Ji-renet, Y. 1989. A true single-phase-clock dynamic CMOS circuit technique. IEEE Journal of Solid-State Circuits, 24(2): 62-70.

Pelleranoet, S., 2004. A 13.5-mW 5 GHz frequency synthesizer with dynamic-logic frequency divider IEEE Journal of Solid-State Circuits, 39(2) : 378–383.

Luca Ciccarelli, Andrea Lodi and Roberto Canegallo, 2004. Low Leakage Circuit Design for FPGAs. In the Proceedings of the IEEE Custom Integrated Circuits Conference, 715-718.

Anderson, J., F. Najm, 2009. Low-power programmable FPGA routing circuitry. IEEE Transactions on VLSI, 17(8): 1048-1060.

Anderson, J. and F. Najm, 2004. Low-power programmable FPGA routing circuitry. In the Proceedings of the 2004 IEEE/ACM International Conference on Computer Aided Design, SanJose, CA, 6020-609.

Navid Azizi and Farid, N. Najm, 2004. An Asymmetric SRAM cell to lower Gate Leakage. In the Proceedings of the 5th International Symposium on Quality Electronic Design, IEEE, 534-539.

Mingjie Lin and Abbas El Gamal, 2008. TORCH: A tool for segmented routing channel design in FPGAs. In the Proceedings of the 2008 ACM/SIG Conference, 131-138.

Li Shang and Alireza, S. Kaviani, 2004. Dynamic Power Consumption in Virtex™-II FPGA Family. In the Proceedings of the International Conference.

Shang, L., A. Kaviani, K. Bhathala, 2002. Dynamic power consumption in the Virtex-II FPGA family. In the Proceedings of the 2002 ACM/SIGDA International Symposium on FPGA, 157-164.

Sundar Prakash Balaji Muthusamy and S. Vijayan, 2012. Low-power optimization in FPGA routing circuits European Journal of Scientific Research, 86(2): 209-217.