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Efficient reduction of power consumption using Cluster based Clock Control Strategy - CCCS

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ABSTRACT

Recently, the reduction of power consumption has become a critical task in the integrated circuit design for impacting the performances of the system reliability and chips. The integrated circuit density is reduced by power reduction and the current resistor drops will make logic failures. In this paper, a clock control strategy is implemented in VLSI circuit for power reduction. The analysis of clustering system and the circuit slack values are taken. The ideal cluster of the circuit is defined by the proposed approach in an efficient manner and the path is defined based on the slack values and delay. In clustering, the maximum phase shift is applied to clock and the circuit design is proposed based on the delay and the performances of the system.By re-scheduling process of the proposed approach is carried out for power consumption. From the IC power consumption, various clocking styles are applied for the peak power reduction and RMS current is reduced with this for the circuit efficiency and performance. The simulation results are carried out by implementing the proposed approach in Cadence Virtuoso Tools. The results are obtained by testing with various processors and slack values of the circuit. It indicates the peak power reduction at least 80% based on clusters and defines the phase-shifted clock of the proposed approach.

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INTRODUCTION

In modern development of VLSI technology and circuit includes more transistor and demand of System On Chip (SOC) in order to incorporate novel architectural features which leads to the power dissipation risk in a expire. Nowadays, clients required a handheld device (like a tablet PC, smart phone) and portable to have long life time on battery. Consequently, power dissipation has become a key issue in VLSI circuits. In the modern world, energy disaster presence becomes extreme fear and the producers cannot afford unnecessary power leakage from a chip. The high power dissipation leads to unnecessarily device heat up forthe reduction of durability, performance and reliability. So the need of low power techniques of VLSI circuit has been increased day to day. The efficient reduction of power dissipation of the circuits is needed while forwarding with more demands of features in a single expires (Mohanty, S.P. and N. Ranganathan, 2004).

Clustering is used to combine the groupsof patterns or spitted sets into disjoint clusters. Such cluster patterns are fitting to various clusters. Clustering is a vital process in many applications like AI, neural network and statistics. It defines the domain with the function for detecting clusters. Clustering procedures are frequently valuable in several application fields such as learning theory, visualization, computer graphics and pattern recognition. A classical vector quantization issue is generally resolved as a gradient-descent problem. However, in repetition a more suitable computing system is a bunch of computation, commonly termed as the K-means algorithm (Andy, M. *et al*., 2006). The k-means method is evaluated and shows the efficiency of clustering results for various applied applications. However, a direct process of k-means method needs the proportional of time for the pattern product and clusters for each iteration. This is computationally very exclusive, particularly for large datasets.

The propagation of portable systems and the platform of mobile computing have been needed for the integrated circuit design with low power consumption. The low power design becomes a vital role and issue in the advance technology to have improvement in the frequency of the clock and the density of the chip. The low consumption of the VLSI design is supplementary determined by several

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factors like environmental worries and thermal deliberations.In portable systems ofbattery driven consists the constraints like peak power, peak power differential, cycle difference power, energy and average power which issimilarly critical part in the design.

The common strategy used for the distribution of clock is consisted with the insertion of buffers with the path and take place change over to flip-flops from the clock source. In a modern VLSI circuit, it forms as a structure of buffered-tree. Each clock signal transition changes the capacitive each node state within the tree flow of clock and dissimilarity with the swapping action in combinational block (Park, S. and K. Choi, 2001; Wu, T.-Y., *et al*., 2010). Also the logic states change is based on the logic function. In low power VLSI design, the total and peak power of the system is similarly restricted in the critical design using the technology of nanometer and deep sub-micrometer. For the peak power reduction the voltage supply level is needed to maintain and required to improve the reliability. For average power and energy reduction needed to enhance the noise margin and lifetime of the battery. Also, required to reduce the energy and coolingexpensive (Hyman, R., *et al*., Saraju, P., *et al*., 2003; Kao, J.T. and A.P. Chandrakasan, 2000; Berger, I., *et al*., 2010).

In the following sections, the rest paper is organized with the reduction of power dissipation of the circuit. In Section II, the survey of the low power design circuit and reduction of power and noise immunity is discussed. The proposed approach explanation and the implementation are carried out in section III and the implementation is in section IV. In section V, the simulation results of the proposed approach and the comparison of performances is discussed. Finally, the proposed approachis concluded with the future works is presented in section VI.

Related Work:

In this section, the literature survey of the clustering approach and its related methods used for power reduction is discussed. In paper (Elias Ahmed and Jonathan Rose, 2004), authors revisited the field-programmable gate array (FPGA) architectural issue of its density and performances with thefunctional effect of logic block. This paper is mainly focused to determine the effect of number of inputs to the LUT in a homogeneous architecture and also to determine the performance of the clustered LUTs and density of an FPGA. First, the architectural results presented in this paper are dependent on the quality of the CAD tools used in the implementation flow. While one of the tools comes with a good optimality result (the Flow map Technology mapper guarantees a depth-optimal LUT mapping) but the majority of tools have heuristic algorithms with no guarantees. Secondly, the results depend directly on the nature of the benchmark circuits they employed. The general clocking sequence of the circuit is shown in Fig (Elias Ahmed and Jonathan Rose, 2004).

The level set methods are presented to recognizethe peak density and valleys in the landscape density for clustering the data. The methods depend onproceeding contours to form the cores of the clusters. One important factor, is that during contour advancement, smoothness can be enforced using LSM. Another factor is that, by using the cluster intensity function, clusters are captured which serves as a form of regularization. Therefore the usual problem of roughness of density functions is overcome. Our method can also identify outliers effectively. After the initial cluster core contours are constructed, outlines are clearly exposed and identified easily. In this method, different contours evolve independently (Andy, M. *et al*., 2006).

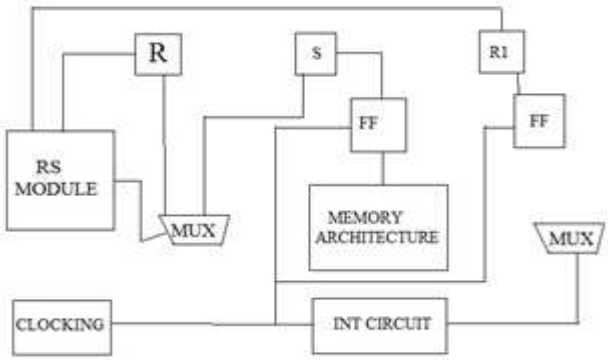

Fig. 1: Clocking Sequence

To discover the subspace clusters, novel subspace clustering models is proposed. In the previous works lack of considering the critical problem, called “the density divergence problem,” in discovering the clusters in subspaces, they consumethe density threshold from the complete density value to recognize the dense regions (Yi-Hong Chu, *et al*., 2010). As per the density

divergence issues, the subspace of the dense region is identified and discovered the clusters with the similar density for the subspace comparison and evaluation of average region density.

In paper (Xiao-Feng Wang and De-Shuang Huang, 2009; Glory H. Shah, *et al*., 2010), using the level set method a novel density-based clustering framework is proposed. Our framework successfully extends the image segmentation method, which is a geometric active contour model of the level set method for data clustering by adopting the cluster centers in data space and it is regarded as the target objects in an image space. Unlike traditional level set methods, the level set evolution scheme can automatically compute the initial boundaries based on Laplacian of probability density function of the data set. To create the signed distance function for level set function initialization, Voronoi source scanning method was used.

A novel density-based network clustering method, called graph-skeleton-based clustering (gSkeletonClu) was proposed. The clustering issues can be renewed to detect the components of the core connectivity in tree structure, by projecting an undirected network to its maximal spanning tree of core-connected.The density-based clustering of a detailedconstraint setting and thestructure of hierarchical clustering are efficiently extracted from the tree. Moreover, desired parameter can be selected in a convenient way to achieve the meaningful cluster tree in a network (Jianbin Huang, *et al*., 2013).

In paper (Le Yu, Bin Wu and Bai Wang, 2013), proposed a Latent Dirichl*et al*location (LDA)-Based Link Partition (LBLP) method, which can find communities with an adjustable range of overlapping. This method employs the LDA model todiscoverthe partitions of link to compute the belonging factor of the community for each link. On the factor basis, the bridge links partitions are defined efficiently. It was validated in the effectiveness of the proposed solution by using both real-world and synthesized networks.

The survey of data clustering algorithms was presented. Each algorithm is unique with its own features. It is easy to understand the clusters which are formed based on the density and these clusters do not limit itself to the shape of clusters. The density of each object neighbors with Midpoint's had been calculated. The change in clusters will occur only in accordance with the changes in density of each object neighbors. The neighbors of each object are characteristicallyresolute using a distance function like Euclidean distancemethod (M.Parimala, *et al*., 2011; Handl, J. Knowles, and D.B. Kell, 2005).

To overcome the disadvantages of DBSCAN and K means clustering algorithms, the density based k-means clustering algorithm has been offered. The result obtained was an improved version of K means clustering algorithm. This algorithm performed better than DBSCAN while handling circularly distributed data point's clusters and also the clusters which are slightly overlapped (Rahmat Widia Sembiring and Jasni Mohamad Zain, 2010).

The proposed approach is used to expand the performance of DBSCAN algorithm. As the Region Query operation takes a long time to process the objects, only few objects were reflected for the enlargement and the remaining missed border objects are handled otherwise during the development of the cluster. Eventually the analysis of the performances and the results of cluster show that the proposed solution was better to the existing algorithms (Mumtaz, K. and Dr. K. Duraiswamy, 2010).

In paper (Hencil Peter, J. and A. Antonysamy, 2010), it was introduced as an EM-style algorithm, namely, Modal EM (MEM), which is used for finding local maxima of mixture densities. For a given data set, it modeled the density of the data non-parametrically by using kernel functions. Clustering was performed by associating each point to a mode, which is identified with initialization at the corresponding point. A hierarchical clustering algorithm, HMAC, was developed by gradually increasing the bandwidth of the kernel functions and the modes which are acquired at a smaller bandwidth are treated recursively as points to be clustered when a larger bandwidth is used.

From the paper (Jia Li, *et al*., 2007), in data clustering techniques it was observed that, Euclidian distance time taken is much more than the Manhattan distance, but the number of clusters formed by Euclidian distance measure is more than the Manhattan distance. Similarly, the noise ratio is also greater for Euclidian distance than the Manhattan distance.

Proposed Approach:

In this paper, the proposed approach of peak power reduction and the cluster based clock control strategy is explained. In order to have optimized circuit of low power the elements switching is reduced. By this technique the identification of path is carried out among various paths and processed by the delay and slack values among the path for the switching reduction. The circuit of the proposed approach is structured as graph. From combinational path for each input the time analysis is performed. Based on the obtained delay slacks information the cluster algorithm categorizes the pathand passed to cluster.

For technology mapping, standard cell library is used to convert the input circuit to structural net-list based on 180nm technology. The mapped list generates the graph by connecting the nodes as per the primary input, output, nets, edges and the logic gates. The aim of the work is to process the combinational or sequential circuits and for concerned methods the clustering approach is applied. After the connection of nodes and edges the

dummy node sink and the source are connected to the output and input respectively.

Grouping terms of the Polynomial function:

$$V_x = [(V^{(i-1)} + V^{(i-1)} R_0)/x] \bmod G(y) \quad (1)$$

Where, Vx denotes the voltage variability, V as the difference voltage along the (I-1) terms, G is represented as grouping. In this process the retiming technique is applied to the function of a register and clocking. It assigns the integer values to the system by reformed the function for clock period. The procedure of the primary input and output is carried out as given below.

Input:

1. Sequential design V- G,E,d
2. Target clock period
3. Voltage supply for each period
4. Voltage Supply K (1<=K<=nr). Each values belongs to delay implementation

Output:

In design, the period of the clock is achieved with the functional equivalent design doe the reduction of device power consumption. Based on power consumed, the system delay is evaluated and the node usage of the cluster path also considered.

$$P_{V=} k_0 D_0 f \text{ (out (vdk) 2)} \quad (2)$$

For each node, the minimized period of clock is included and the given a process at the required time of the device process. From system the clock is removed after the process of device. By this the consumption of power is reduced. The analysis of time is evaluated during the execution of the proposed algorithm for circuit graph. The structure of the nodes includes the type of the node with detailed information, capacitance load, input, output, strength and delay. The graph nodes consider the sink, source, primary process of in and out, gate and fan-out. Here the strength depends on the system, synthesize while obtaining the values of delay and load capacitance. It makes graph assembly easier and it extracts the parameter included in the structure. Also, it maps the capacitances and neighbor delay values. The error is calculated as given below.

$$E = [\sum B_j \text{ x } (z\text{-}z_j 1) L_j] \text{Mod M} \quad (3)$$

Also, if|Z|=2q-1then Z=Zi;

The estimation of soft error of the circuit is based on the function of E and Z from the inductance.The circuit output or the processor is connected to various model circuits.

$$F(t) = N\, d2x/dt + B\, dx/dt + kx \quad (4)$$

The output is labeled based on the n^{th} order differential equation.

$$D_{nx}/dt + yn\text{-}1\ dn\text{-}1y/dtn\text{-}1 + ... = b.dr/dt \quad (5)$$

The 2^{nd} order differential equation is given below with respect to equation (Elias Ahmed and Jonathan Rose, 2004):

$$D_{2x}\ (t)/dt2 + a_1 dy\ (t)/dt + ... = r(t) \quad (6)$$

Sampling period for the equation be,

$$D_{2x}(kt)/dt\ 2 + a_1\ dy(kt)/dt + ... = r(kt)\ ;\ k=0,1,2,..n \quad (7)$$

The sampling modelpromotegeneralizationas below,

$$Y(k+2) + B_{,y}(k+1) + A_{0y}(k) = C_{0r}(k+1) \quad (8)$$

Where, A_0, B_0 and C_0 are representing the terms of lexical and K denotes the total cluster ranges (0, 1, 2, 3... n-1). For each primary input to the delay value is computed by operating the clustering approach and the outputs are defined the analysis of time for all connected paths. The timing is correlates with paths and sure the value of timing in worst case. The dynamic programming scheme is used to estimate the values of maximum delay connected with the entire graph node. Once, the values are obtained, then the state of the density level is propagated. The inputs are processed one by one as per the objects of unclassified by finding the power rating, clustering values of slake, etc.

Proposed Clustering Algorithm:

dcluster (F, epsG, Min)
T = 0
For each unvisited point P in dataset F
Mark P as visited
Neighbor= region(P, epsG)
If sizeof(Neighbor) < Min
Mark P as NOISE
ElseT = next cluster
Expand(P, Neighbor,T, epsG, Min)
Expand(P, Neighbor,T, epsG, MinPts)
Add P to cluster T
For each point P' in Neighbor
If P' is not visited
Mark P' as visited
NeighborPts' = regionQuery (P', epsG)
Ifsizeof (NeighborPts') >= Min
Neighbor=Neighborjoined with Neighbor'
If P' is not yet member of any cluster
Add P' to cluster T
Region(P, epsG)
Return all points within P's epsG-neighborhood (including P)

The system of each clock control is given by

$C_{p1} = \sum C_{l1,}\ 0<=j<=n\text{-}1$

$C_{p2} = \sum C_{l2,}\ 0>=j>=n-1$
$C_{p3} = \sum C_{l3,}0<=j>=n-1$

For path clustering, the values are obtained between the pairs of graph nodes and represented in NX matrix which is similar to the total NODE VALUES. If no path between two nodes, then the value is assigned to -1 and makes the elements with delay values. The values are stored in an efficient manner and extract the maximum values using a memorized algorithm. In vector array the max delay values are connected to the corresponding primary inputs and execute the clustering algorithm as given below.

Procedure – Overlap Cluster approach:

Array [0]
Forto do
Set the start time for cluster to ; balanced
End for
Density_Cluster_paths ();
Array[j] = # of inputs placed in cluster
OPTj = n;
Cluster_factor for cluster i;
Whileloop has not competed for iterations
Store current total factor into PF
Choose the largest imbalanced cluster j
Change the start time.
Re-calculate Total and Cluster Factors;
Store current totalfactor in CF;
If then
Previous configuration was better. Choose the next
Else
Current configuration is better.
Repeat While from here
End if
End while
If array[i] == 0 for some then
Delete cluster;
End if

The objective of the clustering algorithm is to cluster the inputs for the circuit minimization of peak power with the analysis of power reduction. The obtained values are associated with the primary input group within the range of same delay. Also, each cluster is grouped into equal size to balance the source. The proposed approach optimizes the balancing of the system with the generation of graphs and the density.

Implementation:

In this section, the implementation and the simulation results of the proposed approach is explained with its performances and comparison. The proposed circuit is implemented in the Cadence Virtuoso tool. Here, the transient and DC analysis is simulatedfor the estimate of power analysis and generates the .sdf files in the segments of the design. In previous methods, the setup was carried out by focusing round the Synopsys Design- Compiler and Primetime-PX power extension software suites. The simulations are performed on the ISCAS'85 benchmarks and a few circuits from Open Cores. The flow work of the proposed approach is shown in Fig (Andy, M. Yip, *et al*., 2006).

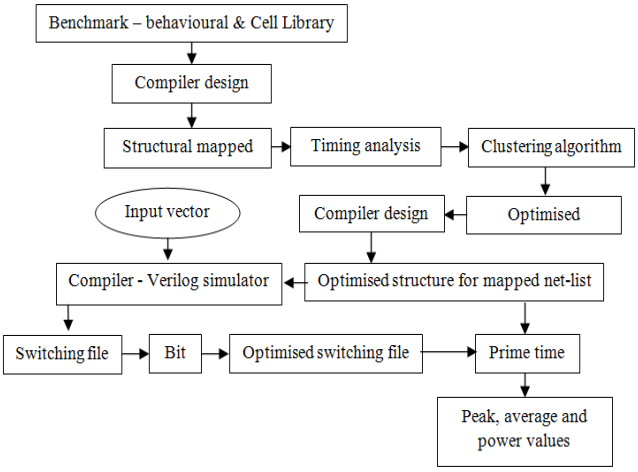

Fig. 2: Flow Work of Proposed Approach

The initial step is synthesizing each benchmark using the standard cell librarytechnology. Whereas, the mapping function is carried out by Cadence VIRTUOSO-180nm CMOS Cell Technology. The input of the proposed path clustering algorithm is the mapped net-list. The clustering algorithm was coded in VERILOG programming language which is further then coded in the Cadence-Digital lab simulation. In the previous method, generated net-list is converted into an acyclic graph structure, but in proposed system direct methodis applied. Where a combinational cell module is characterized by each single node and by each edge the nets arerepresented.

The design Compiler is employed to carry out re-synthesis process.

In this stage, it synchronizes the execution of test vector and attachedthe flip flop modules to the primary inputs. The phase-shifted multiple clocks are generated in various ways with respect to the domain clock. By using counter circuit, decoder logic module is generated based on the strategy of clock divide.

To drive the clock inputs, the clock lines are buffered on the flip flop modules forthe reduction of internal short circuit power. It generated based on large input transition times by the cell modules. The gate-level designs are simulated on the basis of the given resynthesized designs and the standard delay file (.sdf). Alternately, generation of phase-shifted clocks takes place using delay buffers on the original clock. The original clock involves experimentation with many parameters, such as the number of buffers, buffer sizes and the capacitive loads on each clock line. We observed that in a few cases, when buffers are inserted at the HDL level.The proposed system design for the reduction of power is shown in Fig (Yi-Hong Chu, *et al*., 2010).

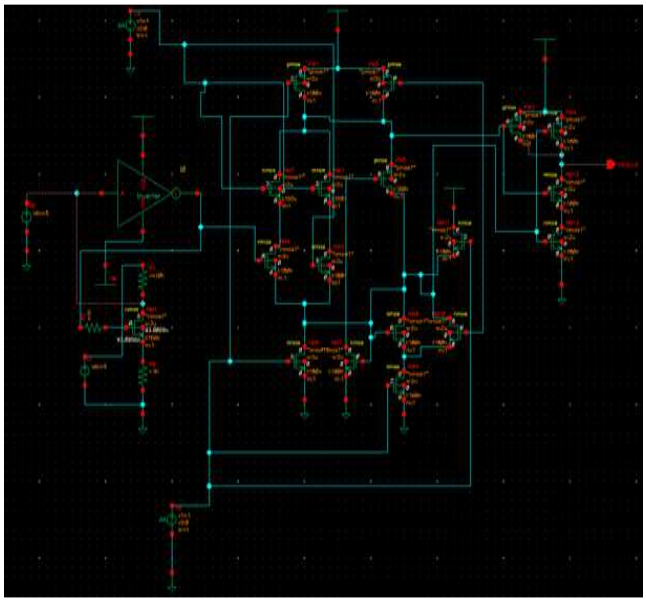

Fig. 3: Proposed System Design

Simulation Results:

The simulation result of the proposed design circuit is carried out in this section. In the set, it includes the single-precision floating-point adder, single-clock divider, ALU core and multiplier from the processor. The simulations were achieved the circuit configurations of traditional clock tree driven circuit and clustering by multiple phase-shifted clock with additional buffering as needed. The reduction of peak-power by clocking scheme is shown in Table [1] in terms of percentage. The mainstream of the circuits have a reduction in peak-power and monotonic peak-power. The average power is obtained using the equation (Mumtaz, K. and Dr. K. Duraiswamy, 2010).

$$Ap=Ap\text{-}dyn+Ap\text{-}static+Ap\text{-}short+AP\text{-}leakage \quad (9)$$

$$Ap\text{-}dyn = Kcfvd2 \quad (10)$$

$$Ap\text{-}short=beta\ f\ (vd\text{-}2Vth) \quad (11)$$

Where, Ap is denotes the average power by removing the dynamic consumption of power at higher state, vth is the voltage threshold, beta is constant, static is fixed and dyn as dynamic. The designed processor is mostly used for testing resolutions. The analysis of DC and transient are specificallyachieved for analysis, in Cadence virtuoso. The system has low power constraint because of a proposed approach sequence of clocking which is capable of providing a reduction in RMS current, total power and peak power. Also, it reduces the complexity of area for less power dissipation. The transient analysis is carried out between the voltage and time (ns). In graph line the linear improvement of the clock is indicatedas per the required of the process and remaining time the clock will be in off condition.

In Analog Design Environment (ADE), the file location is set with its relevant parameters. As per the requirement the cell is extracted. Select Outputs → saveall. The analysis of the power is available in the window of Save Option. From that Select power signal to output by selecting appropriate options of signals. Then click OK for updating the system. As per the simulation of the system the results are obtained by the measurement of power and its

waveform. Also, it ensures the disable of the circuit activities switching. The analysis of static power consumption is shown using the transient response of the circuit in Fig [4].

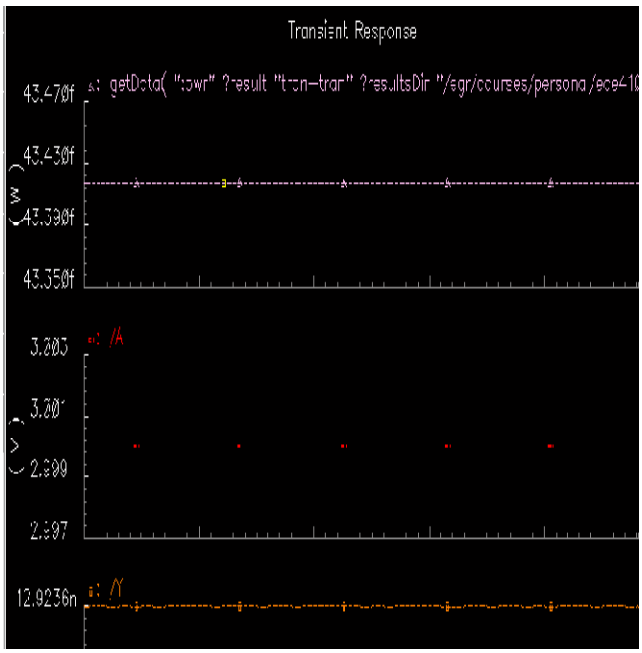

Fig. 4: Transient response of the Static power reduction analysis

An appropriate time range is decided to run a transient simulation of the dynamic and average power accurate measurement. If the simulation length of the transient is chosen too large or small, then it obtains the measurement with the immediate average power value. Also, dynamic power switches the frequency and selects the frequency for the appropriate cycles of the process.

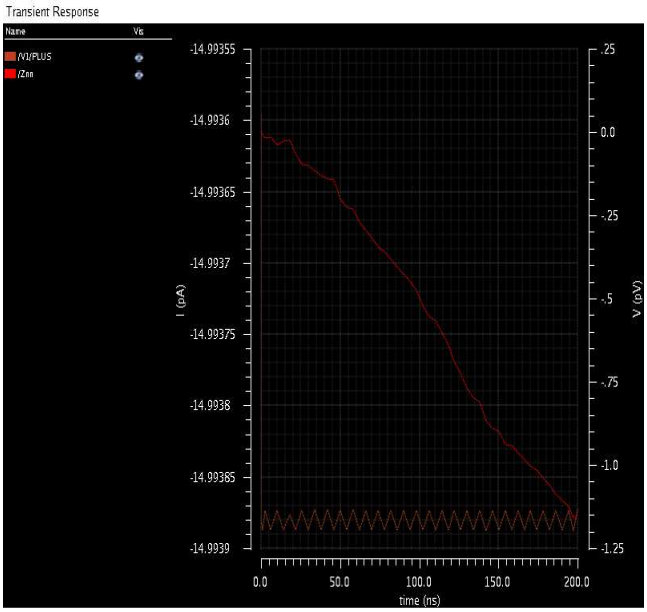

Fig. 5: Transient analysis of dynamic and average power

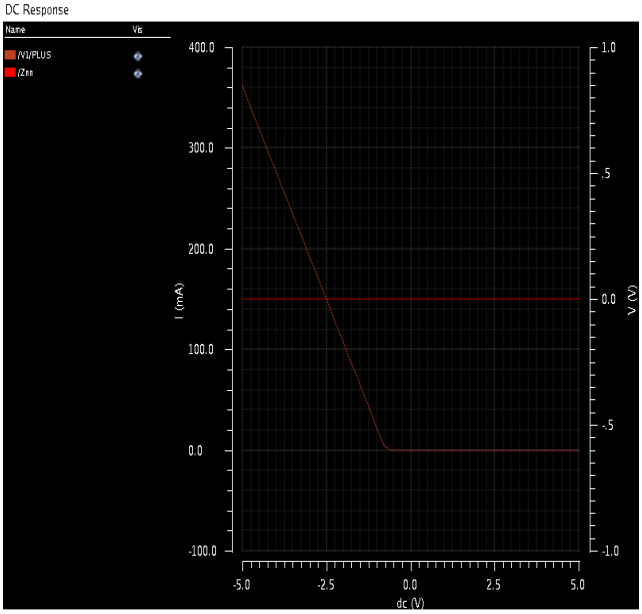

Fig. 6: DC response

Table 1: Performances Analysis of Power and Area of the Proposed Approach

Test circuit	No. of buffers	Total power (mW)	Power over head (%)	Total area (μm^2)	Area over head (%)
C432	3	2.37	3.2	135	4.2
C499	3	2.18	5.3	295	2.98
C880	3	3.45	2.7	298	2.95
Path clustering	7	108.2	5.7	5389	4.1
Proposed circuit	7	102.8	1.65	1402	2.1

The estimation of dynamic power, voltage, logic synthesis and area of the network are processed as per the proposed procedure. The dissipation magnitude is mainly depends on the logic families. Instead of CMOS gates for the power reduction pseudo NMOS is used. Fig [5] shows the transient response of the average and dynamic power of the system.

The transient system response can be changed from stability states and the DC analysis provides scheming for static DC variables. It plots the values from the transfer functions and device IV curves. The graph shows the transient analysis as per the values arrangement in increase manner for the generation of clock. The RMS current is estimated by generating fsdb file using Synopsys Primetime-Power Extension and the evaluation are converted to text file. The RMS value is generated from the text file passed into a VERILOG program and the function is given below.

$$I_{rms} = \sqrt{\int I(t)^2 dt / T} \quad (12)$$

The DC response waveform shows the inverter functions and the circuit operating region to estimate the function under the clock control strategies. The response of DC is shown in Fig [6]. Table [1] shows the performance analysis of the power and area of the various test circuits.

Conclusion:

In this work, clock strategy is presented with the clustering algorithm for the reduction in peak power and analysis of power. The designed circuit considersthe values of slack and inputs to resolutefor analysis. The slacks are sorted in to cluster based density and the path of the clustered circuit is clocked by various styles within the period assigned. Also, based on slack values the phase shift is processed. The proposed clustering approach regulates the path allocation of the clusters to confirmthe distribution of load balancing evenly.The simulation result shows the performances of the peakpower reduction. The proposed work mainly motivated in the analysis of power and reduction of power consumption in VLSI circuits.

REFERENCES

Elias Ahmed and Jonathan Rose, 2004. “The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 12, No. 3, March, pp: 288-298.

Andy, M. Yip, Chris Ding and Tony F. Chan, 2006. “Dynamic Cluster Formation Using Level Set Methods”, IEEE Transactions on Pattern Analysis and Machine Intelligence, 28(6): 877-889.

Yi-Hong Chu, Jen-Wei Huang, Kun-Ta Chuang, De-Nian Yang and Ming-Syan Chen, 2010. "Density Conscious Subspace Clustering for High-Dimensional Data" IEEE Transactions On Knowledge And Data Engineering, 22(1): 16-30.

Xiao-Feng Wang and De-Shuang Huang, 2009. "A Novel Density-Based Clustering Framework by Using Level Set Method", IEEE Transactions on Knowledge and Data Engineering, 21(11): 1515-1531.

Jianbin Huang, Heli Sun, Qinbao Song, Hongbo Deng, Member, IEEE, and Jiawei Han, 2013. "Revealing Density-Based Clustering Structure from the Core-Connected Tree of a Network", IEEE Transactions on Knowledge and Data Engineering, 25(8): 1876-1889.

Le Yu, Bin Wu and Bai Wang, 2013. "LBLP: Link-Clustering-Based Approach for Overlapping Community Detection", Tsinghua Science and Technology, 18(4): 387-397.

M.Parimala, Daphne Lopez and N.C. Senthilkumar, 2011. "A Survey on Density Based Clustering Algorithms for Mining Large Spatial Databases", International Journal of Advanced Science and Technology, 31: 59-66.

Rahmat Widia Sembiring and Jasni Mohamad Zain, 2010. "Cluster Evaluation of Density Based Subspace Clustering", Journal of Computing, 2(11): 1-6.

Mumtaz, K. and Dr. K. Duraiswamy, 2010. "A Novel Density based improved k-means Clustering Algorithm -Dbkmeans", International Journal on Computer Science and Engineering, 02(02): 213-218.

Hencil Peter, J. and A. Antonysamy, 2010. "An Optimised Density Based Clustering Algorithm", International Journal of Computer Applications, 6(9): 20-25.

Jia Li, Surajit Ray and Bruce G. Lindsay, 2007. "A Nonparametric Statistical Approach to Clustering via Mode Identification", Journal of Machine Learning Research, 8: 1687-1723.

Glory H. Shah, C.K. Bhensdadia, Amit P. Ganatra, 2012. "An Empirical Evaluation of Density-Based Clustering Techniques", International Journal of Soft Computing and Engineering (IJSCE), 2(1): 216-223.

Handl, J. Knowles, and D.B. Kell, 2005. "Computational cluster validation in post-genomic data analysis", Journal of Bioinformatics, 21(15): 3201-3212.

Mohanty, S.P. and N. Ranganathan, 2004. "A framework for energy and transient power reduction during behavioral synthesis," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 12(6): 562-572.

Park, S. and K. Choi, 2001. "Performance-driven High-Level Synthesis with Bit-Level Chaining and Clock Selection," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., 20(2): 199-212.

Wu, T.-Y., T.W. Kao, S.Y. Huang, T.L. Li and H.R. Lin, 2010. "Combined use of rising and falling edge triggered clocks for peak current reduction in IP-based SoC designs," in Proc. 15th Asia South Pacific Design Autom. Conf. (ASP-DAC), pp: 444-449.

Hyman, R., N. Ranganathan, T. Bingel and D. Tran Vo, 2013. "A Clock Control Strategy for Peak Power and RMS Current Reduction Using Path Clustering", IEEE Transactions on Very large Integration Systems, 21 (2): 259-269.

Saraju, P., Mohanty, N. Ranganathan and Sunil K. Chappidi, 2003. "Simultaneous Peak and Average Power Minimization during Datapath Scheduling for DSP Processors", ACM digital library, pp: 1-6.

Kao, J.T. and A.P. Chandrakasan, 2000. "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits," IEEE J. Solid-State Circuits, 35(7): 1009-1018.

Berger, I., B. Eldar, G. Zohar, B. Raveh and D. Halperin, 2010. "Improving the quality of non-holonomic motion by hybridizing C-PRM paths," Comput. Res. Repository, abs/1009.4787.