ISSN:1991-8178

Australian Journal of Basic and Applied Sciences

Journal home page: www.ajbasweb.com

Optimized Embedded Adders for Digital Signal Processing Applications

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ARTICLE INFO

Article history:
Received 10 March 2015
Received in revised form 20 March 2015
Accepted 25 March 2015
Available online 10 April 2015

Keywords:
Embedded Logic, Adder, Low power, Modified Booth, XOR gate, Delay

ABSTRACT

Background: Adders are the main element for a wide range of arithmetic units like ALU's and Multipliers. Adder architectures have been under investigation from a very long time, as the critical path determines the overall synchronous system performance used for digital signal processors in embedded applications. **Objective:** In this paper, two Embedded logic Full Adder (PFA-1 and PFA-2) circuits in transistor level is proposed, which reduces logic complexity, gives low power and high speed. The design was implemented for 1 bit and then was further extended till 64 bits. The 1-bit PFA-1 and PFA-2 is designed using 13 and 16 transistors respectively. Also, a 16,32,64 - bit both Linear and Square root Carry Select Adder/Subtractor (CSLA/S) structures are proposed. The proposed adders are compared in terms of PDP and area. Results: While the area for 1-bit PFA-1 is 3.85 $\mu m^2$and for PFA-2 is 4.11μm^2. The PDP of the both proposed adders are 227.75×10^{-18}Ws 306.24×10^{-18}Ws and is compared with the earlier reported designs. Overall delay for CSLA/S is reduced to 75% when compared to conventional one. The implementations are done using Cadence Virtuoso tool with TSMC 32 nm CMOS technology and are found to have power savings of up to 76%.**Conclusion:**The present proposed architectures offers significant improvement in terms of power and speed in comparison to other reported architectures.

To Cite This Article: Kala Bharathan and Seshasayanan Ramachandran., Optimized embedded adders for digital signal processing applications. ***Aust. J. Basic & Appl. Sci.,*** *9(15): 119-124, 2015*

INTRODUCTION

High speed processing capability in tact with low power management is the main strategy for designing arithmetic units for all processors. A Digital Signal Processing (DSP) block involves a wide range of adders and multipliers as basic blocks. Many different design styles are used for implementing strategies, which realize high performance and power efficient full adders. There are various factors, which play a vital role in the optimization of circuit performances like power consumption, noise margins etc. The propagation delay and power is reduced by reducing V_{DD} or by varying the sizes of the transistors along with the choice of logic function and implementation styles.

When devices are cascaded, over consumption of resources occurs. Hence they must be tackled at the fundamental design level. A great improvement to an adder (or any other scalable device) is the reduction of power consumption. One way to reduce the dynamic power consumption of a design is by decreasing the supply voltage.

$$POWER = C_L \times I \times V_{DD}^2 \times f \quad (1)$$

From equation 1, the V_{DD} component is squared, indicating a nonlinear reduction in power per voltage reduction in V_{DD}, which comes at the expense of overall speed and increased delay. In certain cases when V_{DD} is greatly reduced, interference may occur with the logical operations of the circuit. An additional benefit to V_{DD} reduction also comes as improved Power Delay Product (PDP). Many possible techniques are used for transistor optimization process such as buffering, size progression, ordering, etc. The most effective one is the propagation delay and power consumption minimization that comes with the sizing of the transistors. The resistive characteristics of the transistor could be altered with sizing modifications. This decreases the time delay through the device and effectively increases its current driving capabilities, which is given in equation 2

$$T \approx R \times C \quad (2)$$

By setting V_{DD} such that it is increased to boost speed or decreased to improve power conservation and by the lowering of operational clock frequency greatly improves power consumption losses. Also, while making modifications, it is important to

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understand that many tradeoffs occur. With sizing modifications, parasitic capacitances are introduced to act against the optimization gains. The main objective is to build an optimized embedded adder design by reducing the number of transistors. The contributions in this paper is summarized as follows:

1. Two 1–bit full adder structures (PFA-1, PFA-2) with an alternative internal logic consisting of Transmission Gates (TG) and Pass Transistors (PT) for all arithmetic applications are proposed.
2. Minimum sizes on all the transistors are maintained initially and all basic gate structures are modified to reduce the number of transistors when compared to standard ones. The circuits are implemented using Cadence Virtuoso tool with 32 nm TSMC CMOS technology.
3. A 16-, 32-, 64-bit Linear and Square-root Carry Select Adder/Subtractor architecture (CSLA/S) that uses both the PFA-1, PFA-2 as the basic block are proposed.

This paper is organized as follows:

Section 2 presents overall literature survey. Section 3 introduces the alternative proposed embedded logic structure used to build the proposed 1-bit full adders and also explains the Proposed CSLA/S in depth. Section 4 reviews the results obtained from the simulation and the performance comparison done in terms of PDP. Finally, Section 5 concludes this work.

2. Literature Survey:

Static CMOS full adder (A.M Shams, 1999) is based on the regular CMOS structure with pmos pull-up and nmos pull-down transistors. The main advantage of this circuit is its robust structure against voltage scaling and transistor sizing. This circuit provides full swing voltage while the layout is symmetric and efficient due to the complementary transistor pairs. The disadvantage is the large input capacitance due to the large number of transistors and also because of the existence of sized up PMOS transistors its area is affected.

The SR-CPL full adder (Mariano Aguirre, 2011) with swing restoration is another classic circuit. It has both true and complement gate structures with 26 transistors. It provides high-speed and good driving capability due to the level restorers used in the circuit. The SR-CPL consumes large power due to existence of a number of internal nodes and static inverters. These are the main sources for leakage and static power dissipation.

Transmission gate (TG) full adder (Mariano Aguirre, 2011) consists of a pmos transistor and an nmos transistor connected in parallel. TG full adders have no voltage drop problem, are low power consuming and are mainly used for designing xor or xnor gates. The main disadvantage is that they lack driving capability. Hence, in order to improve its weak driving capability, additional buffers are required.

Multiplexer based adder (MBA) (A.Al.Sheraidah, 2004) consists of lesser number of transistors when compared to the static adder but the main disadvantage is it does not operate for low voltage devices.

Dynamic implementations (D3L) (Martin Margala, 2012) on the other hand yields an extremely fast design but end up paying higher costs in the overall power consumption. The full adder functions characterized using the sp-D3L methodology provide the lowest delay and the adder works almost twice as fast as the standard adders selected in the study. The main drawback of these adders is the high power consumption, due to the large number of transistors as well as the multiple paths to ground present in the sp-D3L implementations. This full adder is observed to perform the best when implemented using the concept of propagate and generate signals. This is due to the smaller number of transistors stacked in series and shows the lowest capacitance at the output node. This shows that the capacitance at the output node forms the most critical component of the adder speed irrespective of the number of stages of circuits before getting the sum and carry outputs.

Static Energy Recovery Full Adder (SERF) (E.John, 1999) uses energy recovery technique to reduce power consumption. It is constructed using 10 transistors. Energy recovery logics reuse charge. Therefore, it consumes less energy than the other full adders. Some disadvantages of this circuit are that the sum is generated from two cascaded xnor gates, which lead to long delay. Second, it cannot work correctly in low supply voltage. In the worst case, when $A = B = '1'$ there is $2V_{tn}$ threshold loss in output voltage. The suitable operating supply voltage is limited to $V_{DD} > 2\,V_{tn} + |V_{tp}|$. Second, there are five gate capacitances on a particular node, which causes longer delay to generate intermediate $A \oplus B$ signal.

ULPFA (Denis Flandre, 2010) is used to design low power xor-xnor gates that are implemented using pass transistors to produce the sum. The previous reported level restorer's drawbacks include delay, noise and powerconsumption that are eliminated when ULPD voltage level restorer is used. This circuit is robust against voltage scaling and transistor sizing. The disadvantages include high input capacitance and high area due to the use of low-mobility large pmos in its structure and also the presence of series transistors in the output port creates a weak driver. To eliminate the additional inverter at the output node, the inputs are given in complemented form. The sum and carry out of the ULPFA is designed using two different logic styles, which gives non-symmetrical and irregular layout.

A 14-transistor full adder that employs more than one logic style for their implementation is reported in Vesterbacka (1999). C.H.Chang, (2003) has proposed a Hybrid Pass-logic with Static CMOS output drive full adder (HPSC). Here xor and xnor

functions are simultaneously generated by pass transistor logic using only 6 transistors. This is employed in CMOS module to produce full-swing outputs of the full adder at the cost of increased transistor count and decreased speed. Hybrid logic styles offers promising performance but these adders suffer from poor driving capability issue and their performance degrades drastically while cascading, unless suitably designed buffers are not included.

3. Proposed Architectures:

3.1 Proposed Full Adder (PFA-1):

In this paper, a transmission gate along with pass transistor concept is used to build a xor gate (J.M.Rabaey, 2001) that is further used to propose a 1- bit Full Adder. In PFA-1, xor gate is the main element responsible for most of the power consumption of the entire adder circuit. Therefore, this module is designed to minimize the power to the best possible extend avoiding the voltage degradation possibility. The general full Adder equations are

$$SUM = A \oplus B \oplus CIN,\ CARRY = [(A\times B) + (B\times CIN) + (A\times CIN)] \quad (3)$$

An alternative method proposed here for expressing the sum and carry of full adder using xor gates only is given as:

$$SUM = A \oplus B \oplus CIN,\ CARRY = [(A \times \overline{F}) + (CIN \times F)] \quad (4)$$

The 1-bit Proposed Full Adder (PFA-1) implemented using equation 4 is shown in Figure 1 has 13 transistors (K1 to K13) comprising of TG's and pass transistors. This circuit gives full swing voltage due to the use of TG for xor gate 1 (K1 to K4) and the parasitic capacitances are reduced due to the minimum sizing of the transistors. It gives the exact output for all the inputs shown in the Truth Table 1. This structure is used to build fast adder circuits and registers. This implementation of xor gate requires only 6 transistors, which is shown in Figure 3.1.1, when compared to standard CMOS structure.

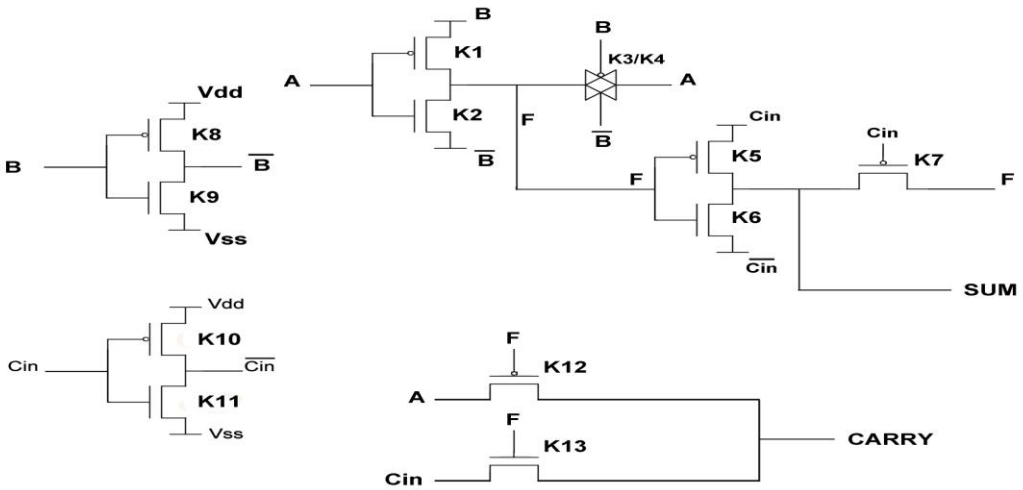

Fig. 3.1: Circuit diagram of PFA-1.

The operation of the xor gate 1 is given below:

i) When B = 1, both the K1 and K2 act as inverter while the transmission gate K3/K4 are off, hence the equation is $F = \overline{A} \times B$ (5)

ii) When B = 0, both the K1 and K2 are disabled and transmission gate K3/K4 are operational, hence the equation is $F = A \times \overline{B}$ (6)

iii) When both the equations are combined at the F node, the respective xor gate 1 output obtained is $F = [(\overline{A} \times B) + (A \times \overline{B})]$ (7)

To build the complete 1-bit full adder structure we use this xor gate 1 output node F as in-out port for the next modules. This F in-out port is further given as one input to the next stage xor gate 2 (K5 to K7), which is implemented using 3 pass transistors only to produce the complete sum of the full adder. This in-out port F of PFA-1 shown in Figure 2.1 produces a strong output voltage (partial Sum) that is used to implement the second stage xor gate 2. Increasing the W/L ratio of transistor K7 minimizes the voltage degradation due to threshold drop. Some of the earlier reported adders are implemented using only pass transistors. This reduces the area and power due to minimum number of transistors but does not produce a strong 1 or 0 at the output node. This becomes a problem when cascading is done for higher bits. Hence the use of a transmission gate to produce the partial Sum (at F node) in PFA-1 provides a strong input for the second stage operation and for the generation of Carry. The XOR gate 2 operates as follows:

iv) When CIN = 1, both the K5 and K6 act as an inverter while the K7 transistor is off, hence the equation is $SUM = \overline{F} \times CIN$ (8)

v) When CIN = 0, both the K5 and K6 are disabled and only transistor K7 is operational, hence the equation is $SUM = F \times \overline{CIN}$ (9)

vi) The SUM of the full adder is obtained by combining above equations

$SUM = [(\overline{F} \times CIN) + (F \times \overline{CIN})]$ (10)

The carry of the full adder is produced using only 2 pass transistors K12 and K13 where the F acts as the control signal. Hence the CARRY expression is

$CARRY = [(A \times \overline{F}) + (CIN \times F)]$ (11)

3.2 Proposed Full Adder (PFA-2):

Another Embedded full adder PFA-2 circuit using 16 transistors is also proposed. Instead of using a pass transistor K7 at xor gate 2, we use a transmission gate. This produces a strong output without any voltage degradation. The working of the circuit is similar to the function of xor gate 1.This is shown in Figure 3.2.1 and the equations obtained are the same.

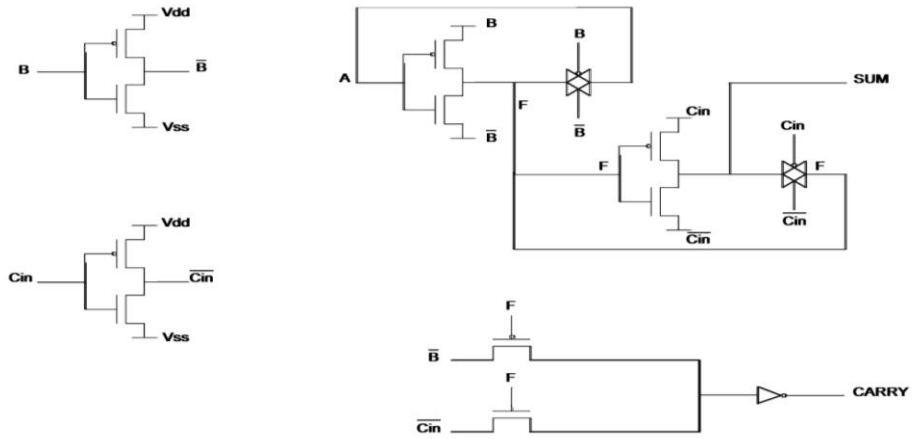

Fig. 3.2: Circuit diagram of PFA-2.

The C_{load} incurs a voltage change ΔV, drawing energy ($C_{Load} \times \Delta V \times V_{DD}$) from the supply voltage V_{DD} for every low-to-high logic transition in an adder. These transitions occur at a fraction αj with the clock frequency fc for each node j belongs to N. The summation of all N nodes in the circuit gives the total dynamic switching power. Hence, transistor size is an effective parameter for reducing dynamic power consumption as shown in equation:

$POWER = V_{DD} \times f_c \times \sum_{j=1}^{N} \propto_j \times C_{Loadj} \times \Delta V_j$ (12)

The inverters have to be weak and the transmission gates have to be strong. The transistor sizes are chosen on the theoretical background of the design initially. Later, the sizes are varied (through simulations) in the vicinity of the previously set values to obtain the best performance in terms of power and delay.

3.3 Proposed Carry Select Adder/Subtractor (CSLA/S):

In digital Adder circuits, maximum time consumed is to propagate a carry output when it is propagated to other devices. In an elementary adder circuit, the sum for each bit position is generated sequentially only after the previous bit position has been summed and a carry is propagated into the next position. A Carry Select Adder (CSLA) is the most challenging one due to its complexity for implementation (B.Ramkumar, 2012). The CSLAstructure is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then selecting a carry to generate the sum. However, the disadvantage of CSLA is that it is not area efficient as it uses multiple pairs of Ripple Carry Adders (RCA). This is used to generate partial Sum and Carry by considering carry input Cin = 0 and Cin = 1. In this paper an approach to optimize the PDP that is energy consumption throughout the entire system design is proposed. The existing standard adder structures are implemented without a Subtractor depending on the application. Here, a Linear and Square-root 16-bit Carry Select Adder/Subtractor (CSLA/S) is proposed as shown in Figure 3.3.1 and Figure 3.3.2. This is extended till 64 bits to test the performance.

The internal modules of CSLA/S are RCA, Binary to Excess-1 Converter (BEC-1), XOR, AND, OR gates. The AND gate is implemented using TG's concept with 4 transistors while the OR gate is implemented using 3 pass transistors with a restorer. Next, a 4-bit Ripple Carry Adder with Half Adder (RCAHA) is designed using 3-bit PFA-1 and 1-bit proposed Half Adder. The 1-bit Half Adder is proposed using 8 transistors. The half adder carry is obtained using TG only and the xor gate 1 is used to obtain the half adder sum. The RCAHA is used

wherever Cin = 0. The ADD/SUB is implemented using XOR gates only and this block indicates a subtraction process only when Cin = 1. This is indicated as the yellow color blocks in Figure 3.2.1 and Figure 3.2.2.The 4-bit RCA block is implemented using 4-bit PFA-1 and PFA-2 circuit. Using BEC-1 instead of Ripple Carry Adder (RCA) reduces the power and area of the Carry Select Adder for the second stage of computation. The main advantage of this transistor level modified BEC-1 is the lesser number of transistors than the ordinary BEC [9]. The Multiplexers (MUX) build using TG is used as final block to select the final sum and carry. Minimum number of transistors for the basic gate structures is maintained throughout the entire design. For the Linear 16-bit CSLA/S, 5-bit BEC is implemented using the proposed XOR, AND gates. For the 16-bit SQRT CSLA/S, different bits of BEC are implemented. Finally, the different bits MUX is build accordingly using TG's. Further to understand the PDP performance the 32-bit, 64-bit linear and square root CSLA/S are also designed and compared with the conventional ones.

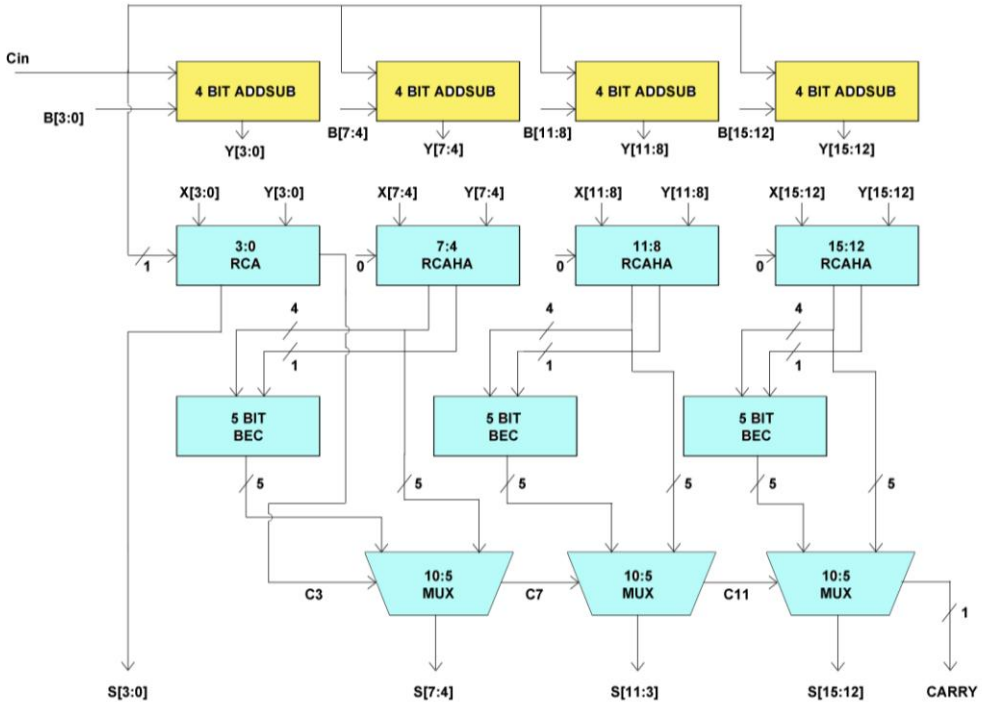

Fig. 3.3.1: Proposed linear CSLA.

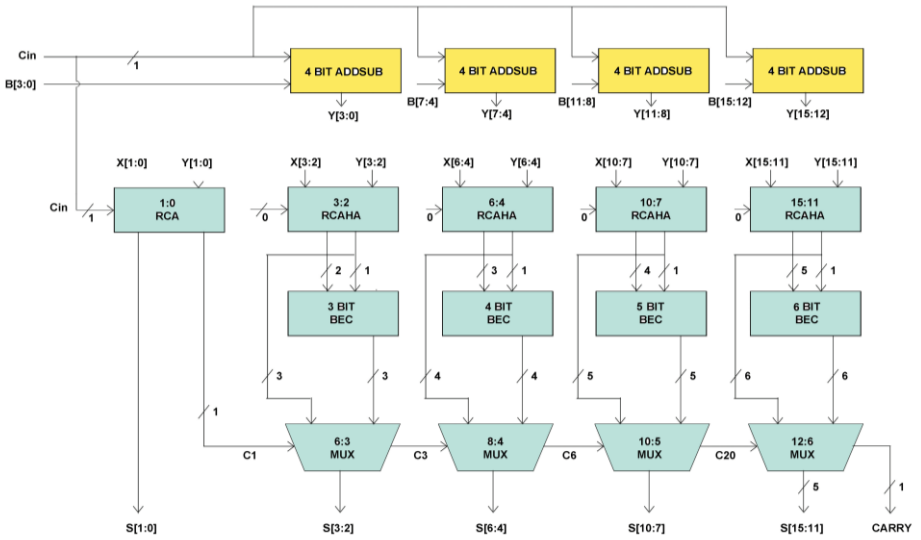

Fig. 3.3.2: Proposed square-root CSLA/S.

4. Simulation Results and Analysis:

The 1-bit PFA-1 and PFA-2 is simulated using several test bench setups. These test benches are having the common prototype of 3 buffers at the input and 2 buffers at the output. The only difference is the number of adder cells stages used in between the input and output of the simulation setup. The number of stages starts from 2 and is increased gradually.

The supply voltage is varied from 1.2 V to 0.7 V for all the different adder structures. The transistor sizes are equally maintained initially and then varied to test the efficiency of the output signals generated for all the full adder circuits. The maximum frequency given to the inputs is 2 GHz for simulations. The performance in terms of power, delay, area and PDP for different full adder structures along with the proposed architectures is compared. The delays reported are the worst-case delays observed in every adder and the average power consumed is obtained for all the possible input combinations as given in Table 4.1.

Considering the power consumption of the whole test bench, the proposed structures shows savings of up to 76%, which is obtained from the overall reduction of dynamic and leakage power components shown in Table 4.1. Due to the combined reduction of power and delay, the PDP obtained is less compared to other full adders. From Figure 4.1, it is observed that the power consumption of the proposed CSLA/S is reduced to about 80% in comparison to the conventional Linear and Square-root CSLA/S using PFA-1.

The overall delay for the proposed CSLA/S both linear and square root using PFA-2 is reduced to about 75%, which results to better PDP shown in Figure 4.2. The number of transistors for the proposed CSLA/S is reduced even for basic gates, which enhanced the efficiency of the circuit

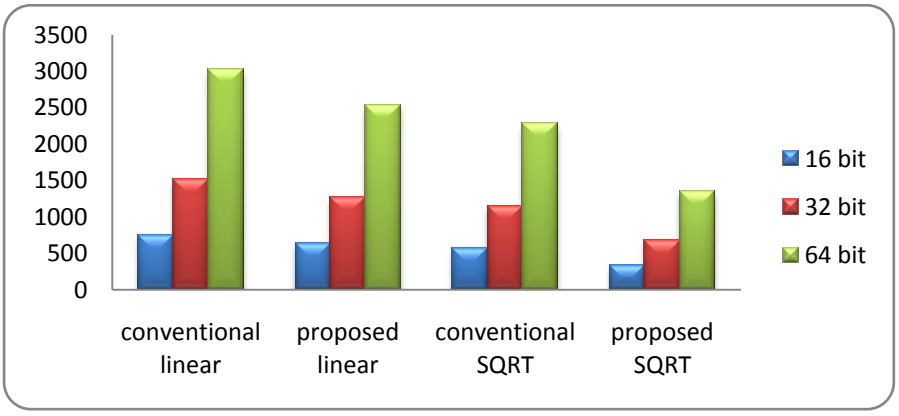

Fig. 4.1: Power variation 16,32,64-bit CSLA/S using PFA-2.

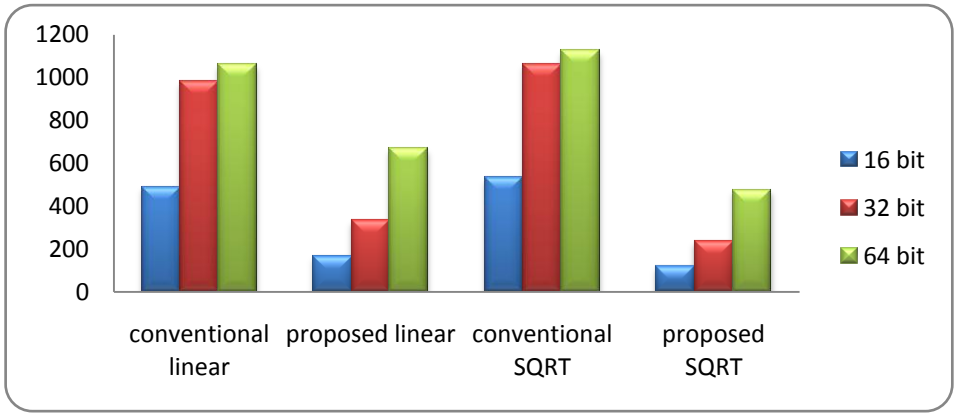

Fig. 4.2: Delay variation for 16,32,64-bit CSLA/S using PFA-1.

Table 4.1: Performance of Different Adders in 32nm Technology.

Adder design	Trans	Delay (ps)	Power (μW)	PDP (10^{-18} Ws)	Area (μm^2)
Static	28	71	15.27	1084.17	7.14
SR-CPL	26	62.5	12.48	780	6.70
Majority	32	105	13.46	1367	8.02
Hybrid	24	60	14.78	886.8	6.26
Mux	20	90	17.97	1617.3	5.38

TG	24	58	16.68	967.44	6.26
$D3L_{pg}$	42	55	14.25	783.75	10.21
10T	10	30	9.87	296.1	3.20
14T	14	28	10.98	307.44	4.07
$sp\text{-}D3L_{pg}$	48	38	26.43	1004.34	11.53
PFA-1	13	25	9.11	227.75	3.85
PFA-2	16	29	10.56	306.24	4.11

5. Conclusion:

Two full adder circuits are introduced in this paper. The proposed 1–bit Full Adders (PFA-1, PFA-2) is built using both transmission gates and pass transistors. The simulations are performed using Cadence Virtuoso tool with TSMC 32 nm LP CMOS technology. This proposed adders are compared against other standard full adders and it shows a 9.71% improvement in PDP compared with earlier best reported. The PFA-1 is extended for 16-, 32- and 64-bits and this was further used as a basic block for designing a Linear and Square-root Carry Select Adder/Subtractor (CSLA/S). The performance of the proposed CSLA/S is compared in terms of speed, power and area with the conventional ones. The proposed CSLA/S shows an area efficient, low power architecture compared to the earlier reported ones. In this paper an attempt has been made to enhance the performance of different architectures used for computations in DSP applications.

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