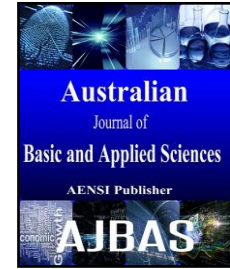




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### Design of SRAM using Multibit Flipflop with Clock Gating Technique

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#### ABSTRACT

In recent trends power plays an key role in VLSI Design. Clock is the major source of power consumption in VLSI circuit. Power consumption is reduced by replacing conventional flipflops using multibit flipflop. Specialized techniques are adapted to merge conventional flipflop into single flipflop. Further clock gating technique is used to improve the power consumption in circuits. Power of SRAM structure using multibit flipflop is compared with the SRAM structure comprises of conventional flipflop structure using Xilinx. This method is used to replace the flip flop and reduces clock power and area by 50%.

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#### INTRODUCTION

Power has become a major source in electronic products. There are four sources of power dissipation in digital CMOS circuits. They are, switching power, short-circuit power, leakage power and static power. The given equation having these four components of power:

$$P_{avg} = P_{switching} + P_{short-circuit} + P_{leakage} + P_{static} \quad (1.1)$$

$P_{switching}$  is the switching power. For a CMOS circuit, the power component usually dominates, and may account for more than 90% of the total power. In this transition activity factor is defined as the average number of power consuming transitions that is made at a node in one clock period. The circuit stored information about the previous history of input is called storage or memory elements. This primitive storage element is constructed from a small number of gates connecting the outputs as an inputs. They have two outputs, one for the normal value and one for the complement value in it. Primitive memory elements is fall into two board classes: latches and flip-flops.

Static power is power consumed while there is no circuit activity. Generally, the power is consumed by a D flip-flop when neither the clock nor the D input have active inputs (i.e., all inputs are "static" because they are at fixed dc levels). Dynamic power is power consumed while the inputs are active. The dynamic power having both the ac component and also static component. As technology advances, a systems-on-a-chip (SoC) design can contain more

and more components that lead to the higher power. So power dissipation reach the limits, cooling or other infrastructure. Reducing the power consumption can enhance battery life but also can avoid the overheating problem increases the difficulty of packaging (Bron, C. and J. Kerbosch, 1973; CAD Contest of Taiwan). Therefore, the consideration of power consumption in complex SOCs has become a big challenge to designers. In VLSI designs, power consumed by clocking is a major part the whole design especially for those designs using deeply scaled CMOS technologies (Chang Y.T., 2010). Thus, several methodologies (Cheon, Y., 2005; Dono, M., 2004) have been proposed to reduce the power consumption of clocking. Clock gating saves power by adding more logic to a circuit to prune the clock tree. It disables the clock gates by AND gate. Switching states consumes power. Not being switched, the switching power consumption goes to zero. The advantage is when the latch is not required to switch state, CLK-gate signal is turned off and the clock is not allowed to charge and discharge  $C_g$ , saving clock power. The drawback is there is area overhead associated with control circuitry. Apart from the latches, it adds some extra AND gates.

To optimize the clock power consumption we introduce the multi-bit flip-flops concept with several techniques. Besides, once more smaller flip-flops are replaced by larger multi-bit flip-flops; device variations in the corresponding circuit can be effectively reduced.

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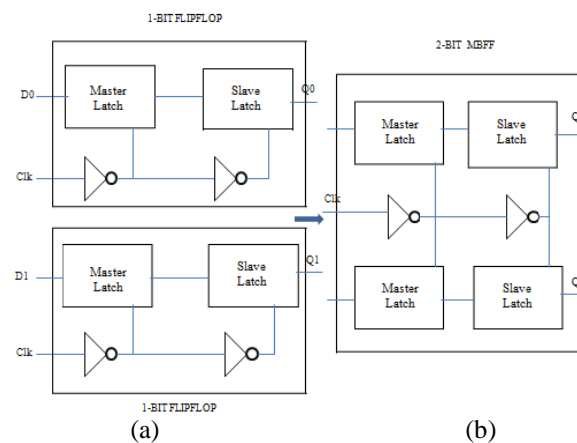
### Existing System:

Clock gating method is well known technique for reduce clock power consumption in circuit. Each circuit varies within and according to their applications, not all the circuits operate at the same time, giving rise to power consumption. By ANDING the clock with a gate-control signal, clock gating effectively disables the clock to an appropriate circuit when the circuit is not in used. So the unneeded power consumption can be avoided charging and discharging of unused circuits. This targets power reduction. In data-driven clock gating, employed for FFs at the gate level, which is most aggressive possible. The clock gating driving a flip-flop is gating when FFs state is not subject to change

in the next clock cycle . It also causes area overhead. So this technique is not effective.

In clock distribution technique, large swing clocking schemes have been proposed. Half swing method needs four clock signal. Due to skew problems among the four clock signal it needs an extra chip. A reduced clock-swing flip-flop requires extra high power-supply voltage to reduce the leakage current .

Another technique called multi-bit flip-flop (MBFF) has recently proposed for clock power reduction. By grouping of FFs, we can reduce the clock power consumption. MBFF is physically merging FFs into a single cell.



**Fig. 1:** Merging of two 1 bit flip-flops into one 2 bit flip-flop (a) Two 1-bit flip-flops (before merging). (b) 2-bit flip-flop(after merging).

The FF grouping problem was NP-hard also occurred first proposed the problem of using multi-bit flip-flops to reduce power consumption in the post-placement stage. Here use graph-based approach is deal with this problem. In this graph, each node represents the flip-flop. If two flip-flops are replaced by a new flip-flop without affecting timing constraints. The graph is built after the problem of replacement of flip-flops. In the graph, this problem can be solved by finding an  $m$ -clique. The flip-flops corresponding to the nodes in an  $m$ -clique can be replaced by an  $m$ -bit flip-flop. It uses branch-and-bound and backtracking algorithm to find all  $m$ -cliques in a graph. Because one node (flip-flop) may belong to several  $m$ -cliques ( $m$ -bit flip-flop), it uses greedy heuristic algorithm to find the maximum set of cliques, in which node only belongs one clique, then finding  $m$ -cliques. If the nodes correspond to  $k$ -bit flip-flops, the bit width summation to flip-flops corresponding to nodes in an  $m$ -clique,  $j$ , may not equal  $m$ . if the library type of a  $j$ -bit flip-flops is not supported by the library, it may be wasting in finding impossible combinations of flip-flops. The following contributions are made in this

To ease the identification of mergeable flip-flops, we find which of the FFs has same clock .Then we find out the same clocked FFs.

Build a combination table before merging two flip-flops, by this we can avoid wasting time in finding impossible combination of flip-flops.

A chip is partitioned into several sub regions and performs replacement in each sub region to reduce the complexity. This may degrade the solution quality. To resolve it, we use a hierarchical way to enhance the result.

### Problem Formulation:

Before solving the problem formulation, a cell library  $L$  and a placement which contains a several number of flip-flops are given to merge the flip-flops as many as possible in order to reduce the total power consumption. If we want to replace some flip-flops by a new flip-flops constraints will occur. Besides, since the replacement would change the routing length of the nets that connect to a flip-flop. Finally, to ensure that a legalized placement can be obtained after the replacement. Then consider this issues, we define two constraints given below.

- Timing Constraint for Net Connecting to a Flip-flop.

- Placement Capacity Constraint will occur. To avoid these problem number of several techniques are proposed in Multi-bit flip-flops.

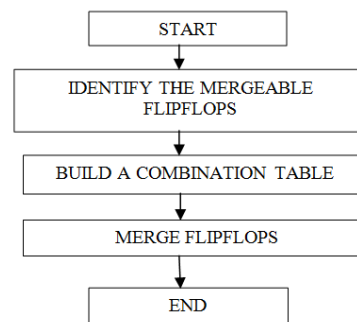
#### **Proposed System:**

##### **Multi-Bit Flip-Flops:**

Reducing clock power and decreasing the total flip-flops by using number of techniques merging multi-bit flip-flops in static RAM.

##### **Flow Chart:**

Our design flow [see Figure 2.] can be roughly divided into three stages. In the beginning, we have



**Fig. 2:** Flow chart.

Thus, we have to combine several bins into a larger bin and repeat this step until no flip-flop can be merged anymore.

##### **Identifying the Merge able Flip-Flops:**

The replacement of some flip-flops with multi-bit flip-flops would change the routing length of the nets that connect to a flip-flop; it inevitably changes timing of some paths. To avoid that timing is affected after the replacement, several techniques are used. First, identify the flip-flops by clock synchronization in circuits. The clock distribution network distributes the clock signal(s) from a common point to all the elements. Since this is vital to the operation of a system, having large attention given to the characteristics of the clock signals and the electrical networks used in their distribution. Clock signal often regarding as a simple control signal; so, these signals are having very special characteristics and attributes.

Clock signals are typically loaded with the largest fan-out and operate at the higher speed of any signal within the clocked system. If the data signals are provided with the temporal reference by the clock signals, the clock waveforms must be clean and sharp. Since these clock signals are again affected by technology scaling, the global interconnect lines become importantly more resistive as line dimensions are decreased. since, this increased line resistance is the primary reason for increasing significance of clock distribution. Atlast,

to identify the flip-flops which of the clock pulse are synchronized in the same region. In the second stage, to build a combination table, defines all combinations of flip-flops in order to get a new multi-bit flip-flop provided by the library. The flip-flops are merged with the help of table. After the legal placement regions of synchronized flip-flops are found and the combination table is built, use above technique to merge flip-flops. To speed up the process, divide a chip into bins and merge flip-flops in the local bin. The flip-flops in the different bins are mergeable.

the control of uncertainty in the arrival times of the clock signals can severely limit the maximum performance of the entire system.

In a synchronous digital system clock signal is used to synchronize the movement of data within the system. Clock signals are required to be distributed at physically remote locations of an integrated circuit. Clock signals transitions drive all the synchronous elements of a digital circuit like Flip Flops and Memories. These elements are referred to as Sinks. Clock Distribution Network (CDN) is circuits that distribute a clock signal from a central global clock source at the centre of the Integrated circuit to all the sinks which use it.

In the process of Clock distribution, the clock signal traverses through a lot of interconnect networks and buffers which are a part of the clock distribution network. These elements introduce delay in the clock signal path. Ideally, a clock signal should arrive at all the sinks at the same time. But due to the variations in parameters like wire interconnect length, temperature variations, capacitive coupling and process variations; the arrival time of the clock transition at different sink locations varies. This spatial variation in the arrival time of the clock transition on an integrated circuit is commonly referred to as Clock Skew. For two points  $i$  and  $j$ , if the arrival times of the clock signals are  $a_i$  and  $a_j$  respectively then the clock skew between two points is given by  $d(i,j) = a_i - a_j$ . The Figure 3. illustrates the reason for clock skew.

Clock signals typically have the highest fan out and operate at the highest speeds in a synchronous digital system. Since the clock signals are used to synchronize the operations of the entire digital circuit the clock transitions should be sharp and should have minimum possible skew to avoid any data integrity errors. As the frequency of operation

of the synchronous circuit increases the circuit becomes more and more susceptible to clock skew i.e. the timing becomes more and more critical. By differential circuit XOR gate, find the difference of clock pulse of each flip-flop. By compare with the reference clock value of the difference is calculated.

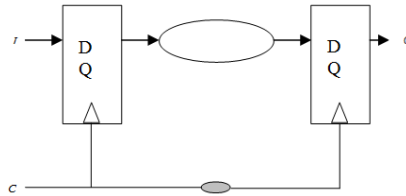


Fig. 3: Clock skew illustration.

**Build a Combination Table:**

If we want to replace several flip-flops by a new flip-flop  $f_i$  (note that the bit width of  $f_i$  should equal to the summation of bit widths of these flip-flops), to make that the new flip-flop  $f_i$  is provided by the library  $L$  when the feasible regions of these flip-flops overlap. Now a combination table is to be built, which records all possible combinations of flip-flops to get

feasible flip-flops before replacements. Further, we can replace flip-flops gradually according to the order of the combinations of flip-flops in this table. We build a combination table, which records all possible combinations of flip-flop to get feasible flip-flops before replacements. Since, it is possible that only one combination of flip-flops needs to be considered each time and also reduced greatly.

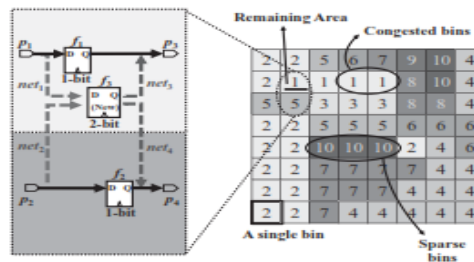


Fig. 4: Combinational of flip-flops in CDN.

Thus the Figure 4 shows the clock distribution network with number of sub regions. Each region operates at different clock pulse. The arrival time of each clock pulse compare with the main clock pulse of CDN. Each flip-flop acted at different clock zone. The clock difference is calculated by the differential circuit. The differential circuit is XOR. By using

reference clock, each flip-flop clock difference is compared and counted. In this section, we illustrate how to build a combination table. Figure 5 shows difference of clock pulse value, from those same bins capable of merging the flip-flop. Initialize the library  $L$  and combinational table.



Fig. 5: Example of library L.

For example consider the library  $L$  that provides 2 types of flip-flops, whose bit widths are 1 and 4 in Figure5. We first initialize two combinations  $n1$  and  $n2$  to represent these two types of flip-flops in the table  $T$  [see TableI(a)]. Next, the function is performed to check whether the flip-flop types between 1 and 4 exist or not. Now, for each

combination in  $T$ , we will build a binary tree as 0level, and root of binary tree denotes that combination. Next, we try to build new legal combinations according to the present combinations. By combing two 1-bit flip-flops in the first combination, a new combination  $n3$  can be obtained [see TableI(b)]. Similarly, we can get a

new combination  $n_4$  ( $n_5$ ) by combining  $n_1$  and  $n_3$  (two  $n_3$ 's) [see Table I(c)]. Finally,  $n_6$  is obtained by combining  $n_1$  and  $n_4$ .

Thus two kinds of flip-flops whose clock rates are equal are added into library L. In below

Library L		Combinational table T	
Type 1	Type 2	n 1	n 2
1 bit	4 bit	1 bit	4 bit

(a)

Combination table T		
n1	n2	n3
1 bit	4 bit	2 bit n1+ n1

(b)

Combinational Table T					
n1	n2	n3	n4	n5	n6
1 bit	4 bit	2 bit	3 bit	4 bit	4bit
		n1+	n1+	n3+	n1+
		n1	n3	n3	n4

(c)

Combination table T			
n1	n2	n3	n4
1 bit	2 bit	3 bit n1 +	4 bit n3 +
		n1	n3

(d)

Table I. Example of building combination table (a) initialize the library L and combination table T.(b) new combination  $n_3$  is obtained from combining two  $n_1$ s. (c) New combination  $n_6$  is obtained from combining  $n_1$  and  $n_4$ . (d) Last combination table is obtained after deleting the unused combination in (e).

To speed up our program  $n_6$  is deleted from T rather than  $n_5$  because its process is longer. After this change  $n_4$  is unused combination. So after deleting  $n_6$ ,  $n_4$  also need to be deleted. Table I(d) as given the last combination table T.

### Merge Flip-Flops:

After the combination table is built the combination of flip-flops are used for merging. That reduces complexity of the whole placement region is divided into several sub regions. Then, several sub regions are combined into a larger sub region and the flip-flops are replaced. Those flip-flops in the corresponding sub region can be replaced further. At last, that flip-flops with the pseudo types can be deleted in the last stage because they are not provided by the supported library.

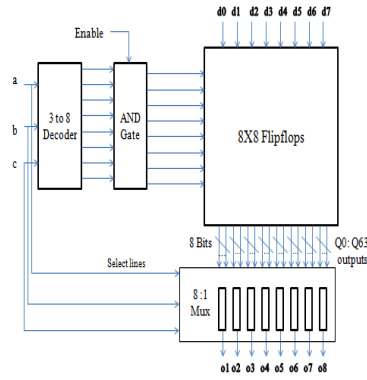
combinations  $n_5$  and  $n_6$  are duplicated because they both represent the same condition, it replaced by combining four 1-bit flip-flops by a 4 bit flip-flop.

1) *Region Partition*: To speed up the process, divide the full chip into several sub regions. By suitable partition, the computation complexity of merging flip-flops can be reduced significantly. Then divide the region into several sub regions, and each having six bins, where a bin is the smallest unit of a sub region.

2) *Replacement of Flip-flops in Sub Region*: Before illustrating the procedure to merge flip-flops, first an equation is given to measure the quality if two flip-flops are going to be replaced by a new flip-flop.

### SRAM Design:

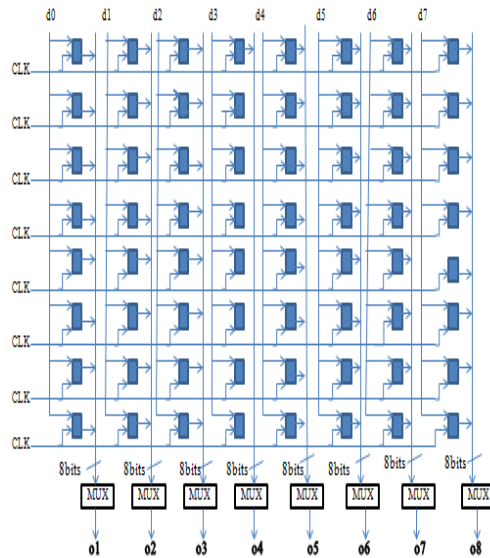
A 8x8 SRAM has been designed which consist of 64 flip-flops in 2D array, it uses 3-to-8 decoder to select a row, a single w/R option is used as both write and read signal, when it is "0" write operation will be performed and when it is "1" read operation is been performed, address line is used to select one of the eight words. According to the algorithm flip-flops whose input does not depend on previous output are the flip-flops that can be merged, without affecting the performance of the design, which uses eight bit flip-flops..



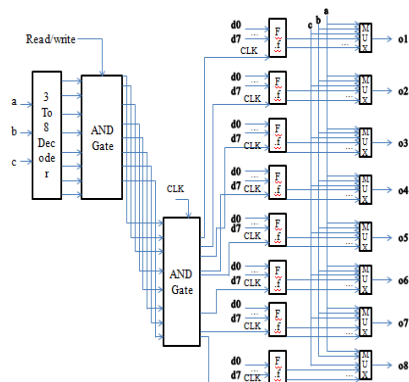
**Fig. 6:** Block Diagram Of Singlebit Flipflop Without Clock Gating technique.

Thus the outputs are obtained in both methods, which does not affect the performance of the original circuit satisfying the proposed algorithm and capacity constraint. A block diagram of single bit flipflop without clock gating technique as shown in

Figure 6. Here internal architecture of 8x8 flipflops as shown above in Figure 7. Figure 8. shows a block diagram of multibit flipflop with clock gating technique.



**Fig. 7:** Internal Architecture Of 8x8 Flipflops.



**Fig. 8:** Block Diagram Of Multibit Flipflop With Clock Gating technique.

## RESULTS AND DISCUSSION

Power results for multi-bit flip-flop are determined using xilinx. The power results for 1-bit, 2-bit and 4-bit flip-flops are obtained and the power consumed by single-bit flip-flop is more than that of

MBFF. Simulation results for merging flipflops of as shown in Figure 9. Simulation results for SRAM structure as shown in Figure 10. The power results and area results for 8X8 SRAM is shown in TABLE II.

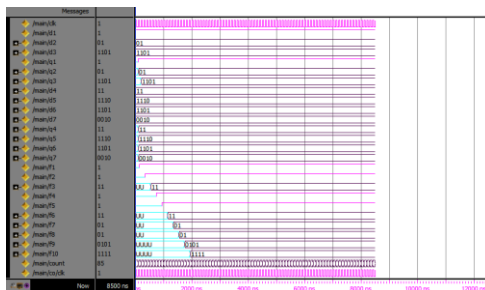


Fig. 9: Simulation Result of Flipflop Merging.

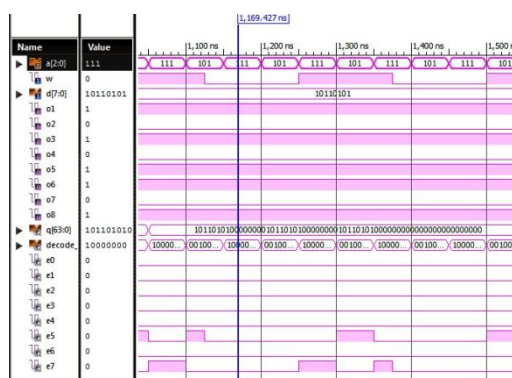


Fig. 10: Simulation Result Of Static RAM Design.

### Comparison Table II:

Table II: Power Results And Area Results For 8X8 SRAM.

Parameter	Single-bit flip-flop	Multi-bit flip-flop
Power(mw)	158	99
Area	14,400	9,648

### Conclusion:

This paper has proposed an algorithm for flip-flop replacement that achieves power reduction in memories and also using clock gating technique it clearly shows that more power is reduced. Therefore, the direct way is to repeatedly search a set of flip-flops that can be replaced by a new multi-bit flip-flop. Thus, it is clearly shows that if the number of flip-flops in a chip increases, the complexity also increases, which makes the method impractical. By the guidelines of replacement from the library, the impossible combination of flip-flops will not be considered since it reduces the execution time. The experimental result shows that our algorithm reduces power. Future work involves design for 8X8 SRAM in cadence EDA tool.

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### REFERENCES

- Bron, C. and J. Kerbosch, 1973. Algorithm 457: Finding all cliques of an undirected graph. ACM Commun., 16(9): 575–577.
- CAD Contest of Taiwan [Online]. Available: [http://cad\\_contest.cs.nctu.edu.tw/cad11](http://cad_contest.cs.nctu.edu.tw/cad11)
- Chang Y.T., C.C. Hsu, P.H. Lin, Y.W. Tsai and S.F. Chen, 2010. Post-placement power optimization with multi-bit flip-flops. in Proc. IEEE/ACM

Comput.-Aided Design Int. Conf., San Jose, CA, , pp: 218–223.

Cheon, Y., P.H. Ho, A.B. Kahng, S. Reda and Q. Wang, 2005. Power-aware placement. in Proc. Design Autom. Conf., 795–800.

Dono, M., E. Macii and L. Mazzoni, 2004. power-aware clock tree planning. in proc.int. symp. Phys. Design, 138-147.

Duarte, D., V. Narayanan and M.J. Irwin, 2002. Impact of technology scaling in the clock power. in Proc. IEEE VLSI Comput. Soc. Annu. Symp., Pittsburgh, PA, 52–57.

Faraday Technology Corporation [Online]. Available: <http://www.faraday-tech.com/index.html>

Gronowski, P., W.J. Bowhill, R.P. Preston, M.K. Gowan and R.L. Allmon, 1998. High-performance microprocessor design. IEEE J. Solid-State Circuits, 33(5): 676–686.

Hou, W., D. Liu and P.H. Ho, 2009. Automatic register banking for low-power clock trees. in Proc. Quality Electron. Design, San Jose, CA, pp: 647–652.