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Mixed Signal Integrated Circuits Testing Using Wavelets And Neural Networks

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ABSTRACT

Fault diagnosis is still increasing area of research as the systems become complex day by day and their complexities are ever growing. Fault detection and identification are important to ensure safety and consistency of practical analog circuits. Fault analysis of digital circuits has stretched the point of computerization, whereas those of analog circuits are still exciting. Diagnoses of such faults are undeniably challenging as well as interesting. In this paper, some new techniques for diagnosing the soft faults of analog circuits have been studied and a method using PSPICE and MATLAB has been proposed.

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INTRODUCTION

Electronic tests are system dependent and are classified as digital, analog and/or mixed-signal. The testing of digital circuits are well established. Methodologies for the testing of analog circuits remain relatively under developed due to the composite nature of analog signals.

Analog and Mixed Signal(AMS) ICs are acquisiting popularity in consumer electronics, biomedical equipment, wireless communication, networking, multimedia, automotive process control and real time control systems. AMS ICs will organize the best part of future electronic devices, making it essential to research AMS testing, which include digital and analog testing lags far behind in both methodologies and tools and therefore demands generous research and development effort.

Majority of the analog circuit testing techniques can be classified as either specification-driven or fault model-driven. In the specification-driven techniques, the correctness of Circuit Under Test (CUT) is verified by checking the set of measured parameters within the tolerance range. The CUT is declared as faulty if any of the measured parameters falls outside the tolerance range. In the fault model-driven techniques, a fault list is first constructed and the fault is declared as detected if the discrepancy between the output of the nominal design and the faulty circuit is greater than certain derived range, which limits come from measurement error, process variation, etc.

Therefore, for fault-model-driven techniques, the observables for the fault detection should be detected carefully such that the deviation caused by the defect can be easily observed and measured.

II. *Classification Of Faults In Analog Circuits:*

Every system is responsible to faults or failures. In most general terms, a fault is a change in a system that prevents it from operating in the proper manner .A fault can be defined as “anything other than estimated behavior ”.Defects in analog circuits can be classified based on the

(i) sequential parameters
(ii) occurrence of defects appearance
(iii) the number of defects present in the device
(iv) the industrial process

Faults may occur in analog circuits in two different ways.

- Catastrophic faults:. The faults include shorts, opens or large variation of the design parameters. Catastrophic faults are caused by major structural distortions or extreme out of range parameters and lead to failures that apparent themselves in a completely malfunctioning circuit.
- Parametric faults: The faults are due to the process fluctuations. These faults involve parameters deviations from their nominal value that can consequently quit their tolerance band.

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III. Importance Of Fault Diagnosis:

Fault diagnosis is often considered to be at two-stage process: First, the fault has happenedmust be recognized which is referred as fault detection. Second, the nature and location should be determined such that appropriate counteractive action may be initiated which is referred as fault identification.

Fault detection in analog electronic circuits is a difficult problem due to a limited number of outputs, inputs and testing signals. Creation of analytical models of circuit faults is difficult due to complex nonlinear dependence between fault types and characteristics of the testing signals.

The complexities in testing of analog circuits are due to the changes in the technological process. Fault detection and identification are important to guarantee safety and reliability of practical analog circuits. Fault analysis of analog circuits is the most important techniques in circuit development stage and in fault analysis stage.

IV *Fault Diagnosis Approaches:*

A.DeterministicandProbabilisticApproaches:

In general, a system can be analysed for faults in the following approaches. The major approach is deterministic in nature consisting of definite component deviation and operating. Even though the deterministic approach is quite accurate, the deficiency of flexibility and adaptability in diagnosing a fault condition is its problem. On the other hand, the probabilistic approach for fault diagnosis is flexible and adaptive, because the components are assessed for the faults based on the failure probability attached to each of the component.

B.Structural and Functional Testing Approaches:

The approaches of analog circuit testing can be divided into two groups namely structural testing and functional testing. In structural testing the tested circuit is considered as “White Box” where as in functional testing the tested circuit is considered as “Black Box”.The main benefits of functional testing are

- Ease of test signal selection during a design stage of devices.
- Support of checking of the output characteristics correspondence to their technical conditions.
- Allows making fault diagnosis.
- Acceptance of integration with methods of digital circuits functional testing.

Functional Testing includes the following shortcomings:

- Difficulties to inscribe test programs
- High dimensions of test vectors for the large circuits
- High computing outlays, etc.

C. Built in Self-Test (BIST) Approach:

The strategies of Built-In Testing are

- On-line (working mode) - Faults are detected during execution by the circuit proposed for it.
- Off-line (dedicated mode) - Tested circuit is substituted to the committed mode, at which the usual operation of the device is impossible.

The differences between BIST solutions are the ways of input test signal variety, the ways of output retorts processing, the choice of restrained parameters and the means of operation. The method of BIST in which the test circuit is built inside the integrated circuit increases the complexity, cost and decreases the speed.

D.Simulation after Test and Simulation before Test:

The Simulation Before Test approach (SBT) and the Simulation After Test approach (SAT) are two major approaches for fault diagnosis of analog circuits. In the SAT attitude, fault diagnosis is obtained by computing the circuit components from the measured responses of the CUT.

The SBT approach compares the circuit responses related with the predefined fault values in the dictionary to locate the faults. This approach confirms a short test time even for complex circuits.

i) Simulation After Test:

The general system of SAT functional diagnosis is given as

- Measuring responses of CUT.
- Calculation (estimation) of components parameters using circuit output responses and known topological structure.
- Decision making about circuit accuracy.

The procedures of SAT testing and diagnosis are

- Symbolic analysis - Tree enumeration methods, Flow-graph methods, Numerical interpolation methods, Parameter extraction methods and Determinant expansion methods
- Artificial intelligence systems – Model based reasoning approach, Qualitative Reasoning (QR) approach and Fuzzy Logic approach
- Parametric identification Model based reasoning works with models describing common structure of the device

ii) ***Simulation Before Test:***

The general algorithm of SBT functional diagnosis consists of the following steps.

- Generation of the faults list
- Attaining output responses of device for these faults
- Construction of the fault dictionary
- Measurement of CUT's output responses on test signals
- Comparison of obtained responses of the CUT with values from the fault dictionary and decision making about circuit correctness.
- Fault detection and isolation is achieved by means of a classification system which makes a decision based on the mark differences between the actual CUT responses and the stored ones.

The following methods are to be followedTo design the fault dictionary,
-a set of suitable input motivations exciting the CUT so as to maximally amplify the presence of faults must be selected.
-a set of output parameter features establishing the fault signatures (e.g. test node voltage magnitudes or phases, current magnitudes or phases) must be identified.

The fault dictionary must be as compact as possible to reduce the complexity of the diagnosis procedure. The problems of fault dictionaries usage are classified as
- High dimensions. The enclosure of large number of output responses results in large expenses of resources.
- Limitations of a set of saved output responses that do not allow analyzing the faults which have not been comprised in the fault dictionary.

The block diagram of the SBT approach is given in Fig.1.1. The SBT approach fault detection includes four basic modules, specifically simulator or acquisition module, pre-processor, feature extraction module and classifier.

PSPICE and Matlab can be used as simulators. The pre-processor module compacts the simulated or measured data into features suitable for classification purpose. Fourier and wavelet transforms are utilized as pre-processors in many research works (et al; Boukhatem, B., 2012). wavelet transform generates a family of hierarchically organized low and high frequency components. Feature extractor creates new features based on the transformations or combinations of the input features. It moderates the classifier charge and improves the classification performance.

Principal Component Analysis (PCA), QR factorization, Bayesian theory, Artificial Neural Networks (ANN) and fuzzy approach are some of the feature extractors. Classifier provides the defective or fault free condition of the CUT. Neural classifier, fuzzy classifier or integration of both can be used as classifiers. The SBT approach is shown in Fig.1. (Czaja, Z., 2007).

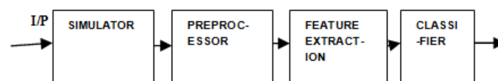

Fig. 1: SBT approach.

V. *Fault Diagnosis Procedures:*

The fault diagnosis procedure consists of three basic steps as shown in Fig.2. The first step is to simulate the Circuit Under Test (CUT) in PSPICE using Monte Carlo analysis and to generate the fault dictionary. The second step is to pre-process the fault dictionary using kernel principal component analysis. Third step is to classify the faults in CUTs using training algorithm.

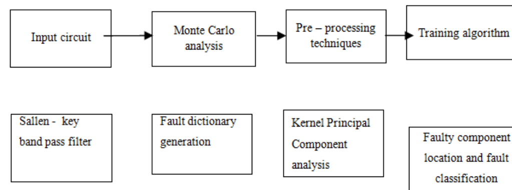

Fig. 2: fault diagnostic procedure.

VI. *Description Of Fault Diagnosis Procedure:*

A. *Input circuit:*

The input circuit taken for testing is sallen-key band pass filter circuit. Fig.3. represents the Sallen-key bandpass circuit.

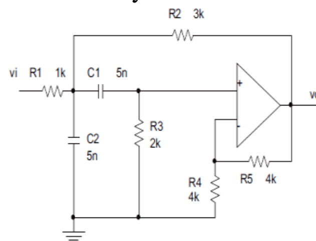

Fig. 3: Sallen-Key bandpass filter.

The circuit designed is simulated in PSPICE to check its correct functionality under normal condition and for their respective fault classes.

B. *Pre-processing techniques:*

i) *Kernel principal component analysis:*

Kernel principal component analysis (KPCA) is

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a technique used to transform candidate features to an optimal set for training the circuit. Given a set of N candidate features to train the circuit for a particular task, KPCA selects M features with M<=N such that the loss of essential information and datavariationrequiredfor classification .is minimized. KPCA achieves this goal by minimizing a measure of the distance such that a pre-specified percentage of the variation in the data set is preserved.

ii)Training algorithm:

Neural networks are applied in all kinds of fields because of many facts such as large scale parallel processing, distributed storage, nonlinear mapping etc. ANNs provide a appliance for adaptive form classification. ANNs are capable of robust classification even in the followingenvironments:

- poorly defined system replicas
- noisy input environments
- nonlinear

VII. ***Simulation Results:***

Monte Carlo Simulation:

Sallen-key band pass filter has been taken as a sample circuit as shown in Fig 4.

The simulation result for No Fault (NF) class is shown in Fig.5.The simulation result for R2↑ (SF1) class is shown in Fig.6.

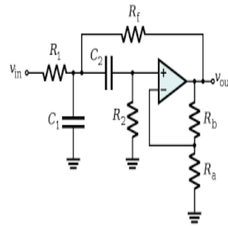

Fig. 4: PSPICE model of sallen-key band pass filter.

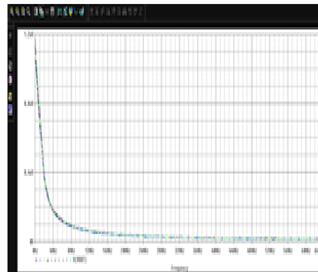

Fig. 5: Monte Carlo simulation.

Kernel Principal Component Analysis:

The candidate features extracted from wavelet transformare further processedby KPCA in order to extract the optimal features used for training the neural network. Two PC corresponding to single fault classification of Sallen- key bandpass filter is shown in Fig.4.3.

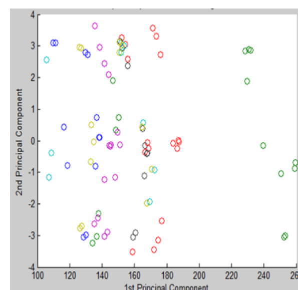

Fig. 6: KPCA for Sallen-keybandpassfilter.

VIII. ***Conclusion:***

In this paper, some new techniques for diagnosing the soft faults of analog circuits have been studied through benchmark circuits and a method using PSPICE and MATLAB have been proposed. The study reveals that the proposed preprocessing techniques have a significant impact on analog fault diagnosis in theselection of the optimal numbers of relevant features.This leads to neural network architectures withreasonable size

and achieve a high degree ofdiagnosis accuracy for various fault classes.

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