



ISSN:1991-8178

Australian Journal of Basic and Applied Sciences

Journal home page: www.ajbasweb.com



Performance Analysis of Different Types of Adder Using 3-Transistor XOR Gate

Lourdy Nivethitha, V. and Jawahar, A.

Department of Electronics and Communication Engineering, SSN College of Engineering, Anna University, Chennai, India.

ARTICLE INFO

Article history:

Received 20 January 2015

Accepted 02 April 2015

Published 20 May 2015

Keywords:

Ripple carry adder

Carry select adder

Carry skip adder

ABSTRACT

An adder is a digital circuit that performs addition of numbers. They are used in ALU's, processors for addition. In this paper different types of adders are designed using three transistors XOR gate and their performances are analysed. In order to reduce the number of components and to improve the performances, an XOR gate circuit is designed using minimum number of transistors. By using this XOR gate, different types of adders like ripple carry adder, carry select adder, carry skip adder are designed using TANNER tool and parameters like delay, average power consumption, area are measured. The obtained performance measurements are compared with performance of adder designed using XOR circuit which has increased number of transistors. The result shows that the carry skip adder has better performance than other adders.

© 2015 AENSI Publisher All rights reserved.

To Cite This Article: Lourdy Nivethitha, V. and Jawahar, A., Performance Analysis of Different Types of Adder Using 3-Transistor XOR Gate. *Aust. J. Basic & Appl. Sci.*, 9(16): 44-50, 2015

INTRODUCTION

Addition is an indispensable operation which is used in many VLSI systems such as application-specific DSP architectures and microprocessors. Adders are used not only for addition, but also the core of many other useful operations such as subtraction, multiplication, division, address calculations, etc. Several algorithms have been presented for high speed parallel addition, and there is generally a trade-off between speed and area. Hence, binary adders are crucial building blocks in very large-scale integrated circuits. Adder is an important part that determines the overall performance of the system so that building blocks of adder cell are improved for better performance. So designers are faced with more limitations: high speed, less area, high throughput and at the same time, low power consumption. So designing low power, high performance adder cells are very important in designing system.

A structured approach for analysing the design of adders is followed. This approach is decomposing the full adder structure into smaller blocks. For optimization of speed in adders, the most important factor is carry generation. For implementation of a fast adder, the generated carry should be driven to the output as fast as possible, thereby reducing the worst path delay which determines the ultimate speed of the digital structure.

A. Related Work:

Design of electronic system with less area, power-efficient and high speed of operation is one the most challenging area of research in VLSI system design. Delay is the time lagged between given input and response. There are different types of delays present in VLSI design. Delay in circuit ruins the performance like speed, accuracy which leads to electronic product useless.

When the number of components increased delay is also increased. So the number of components required to build a system should be taken into account. In recent years different types of adder using different logic style have been propose. Standard CMOS adder with 28 transistors using pull-up and pull-down networks given in (Goel, S., 2006). Transmission gate CMOS adder with 20 transistors is given in (Leblebici, Y. and S.M. Kang, 1999). This adder requires twice the number of transistor used in pass-transistor logic implementation with 32 transistors given in (Muthukumaran, S. and A. Jawahar, 2014) for same logic function. A full adder using transmission function theory with 16 transistors is given in (Shams, A.M. and M. Bayoumi, 2000). Multiplexer based adder with elimination of direct path to power supply using 12 transistors is given in (Weste, N. and K. Eshraghian, 1993). Full adders using 16 transistors with XOR/XNOR design is given in (Yingtao Jiang, 2004). Full adder using hybrid CMOS logic with 22 transistors is given in (Zimmermann, R. and W. Fichtner, 1997).

Corresponding Author: V. Lourdy Nivethitha, Department Electronics and communication Engineering, SSN College of Engineering, Kalavakkam - 603110, India. Phone numbers – 919487947999, E-mail: lourdynivethitha@gmail.com

B. Motivation:

The main motivation of this paper is the miniaturization which is the main requirement of the VLSI design. Miniaturization should be done in terms of less area, low power consumption, high speed of operation, less delay etc. in order to achieve better performance. The full adder is usually a component in a cascade of adders, which add 2, 4, 8, 16, 32, etc bit binary numbers. The function of full adder is based on following two equation, A, B, C_{in} are the three single bit inputs and generates two outputs of single bit Sum and C_{out} where:

$$\text{Sum} = (A \oplus B) \oplus C_{in} \tag{1}$$

$$C_{out} = A.B + C_{in} (A \oplus B) \tag{2}$$

The reminder of paper is organized as follows. In section II design and implementation of ripple carry adder, carry select adder and carry skip adder using full adder were done. In section III performance of different types of adders were compared. Finally in section IV the work was concluded.

C. Design of 8 Transistor XOR Gate:

The CMOS XOR gate is designed using eight numbers of transistors. When the number of transistor increases then area occupied is also increased. Propagation delay and power consumption also get reduced then the adder will work slowly. A CMOS AND, XOR, OR gate which is used to design conventional full adder is shown in Fig.1, Fig. 2, and Fig. 3.

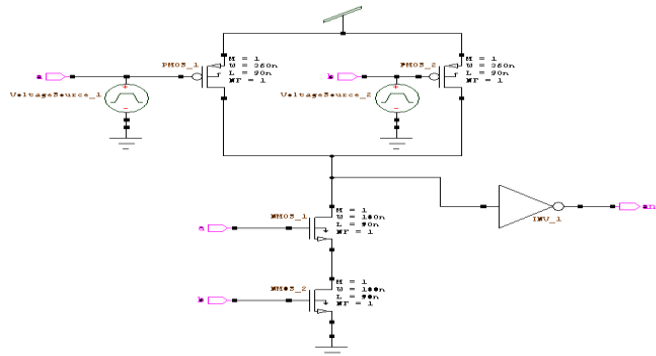


Fig. 1: CMOS AND circuit.

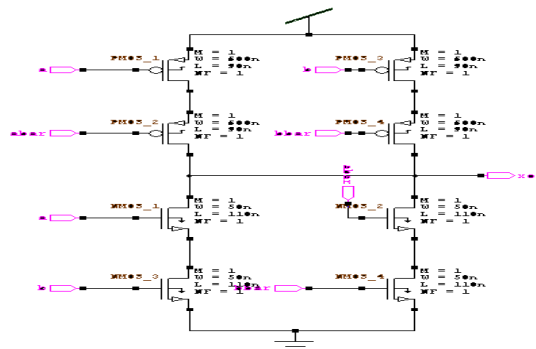


Fig. 2: CMOS 8transistor XOR circuit.

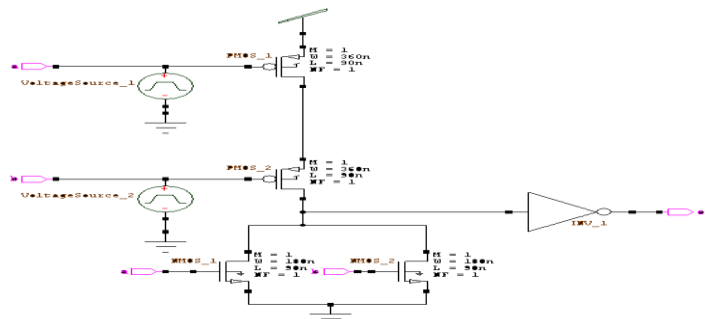


Fig. 3: CMOS OR circuit.

D. Design of 3 Transistor XOR/XNOR Gate:

The design of XOR/XNOR cell is given in (Zhuang, N. and H. Wu, 1992), gate lengths of all

three transistors have been taken as 90nm. Widths of transistors in XOR gate is shown in TABLE I. voltage degradation due to threshold drop can be

reduced by increasing W/L ratio of transistor of NMOS_1. The design of XOR/XNOR circuit using 3- transistors gate is shown in the Fig. 4. The

simulated waveform for XOR/XNOR cell is shown in Fig. 5.

Table I: Width of transistors in XOR circuit.

DEVICE NAME	WIDTH (nm)
PMOS_1	600
PMOS_2	600
NMOS_1	50

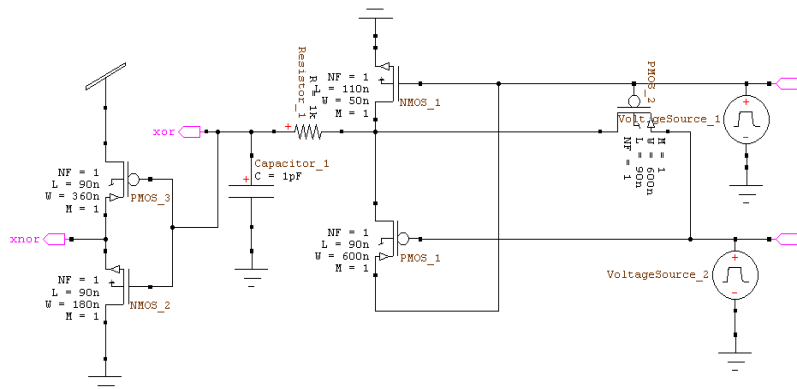


Fig. 4: Design of XOR/XNOR circuit using 3 transistors.

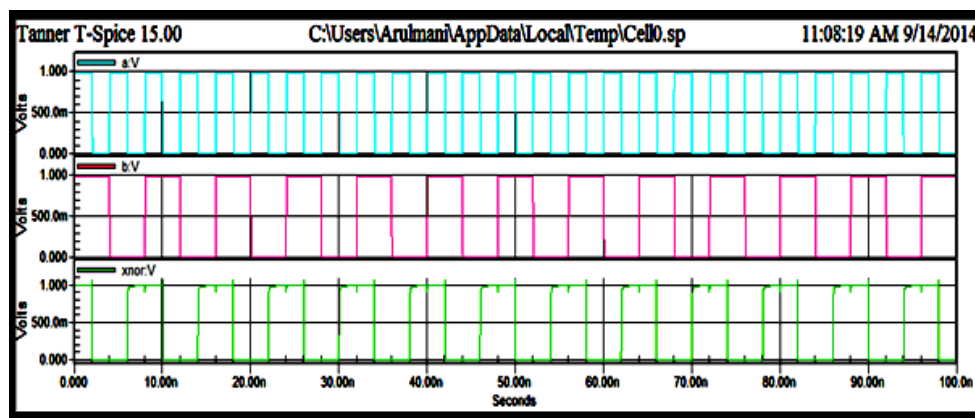


Fig. 5: Simulated waveform for proposed XOR /XNOR cell.

II. Implementation of Different Types Adder:

The design and implementation of ripple carry adder, carry select and carry skip adder are shown below.

A. Full Adder Using 3T and 8T XOR Gate:

The single bit full adder is designed using 3 transistors XOR gate is shown in Fig. 6. The single bit conventional full adder is designed using 8 transistors XOR gate is shown in Fig. 7.

B. Ripple Carry Adder (RCA):

The single bit full adder is connected in cascade manner to determine its driving capability. By using the proposed single bit full adder as a benchmark, 4-bit ripple carry adder is implemented. The schematic diagram for 4-bit ripple carry adder with 4 full adders

is shown in Fig. 8. The simulation output of 4-bit ripple carry adder is shown in Fig. 9.

C. Carry Select Adder (CSA):

It generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry select adder is done with two adders (two RCA) in order or performs the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. For a group, sum and carry is already calculated, simply select based on carry. The schematic diagram of carry select adder is shown in Fig. 10. The simulation output of carry select adder is shown in Fig. 11.

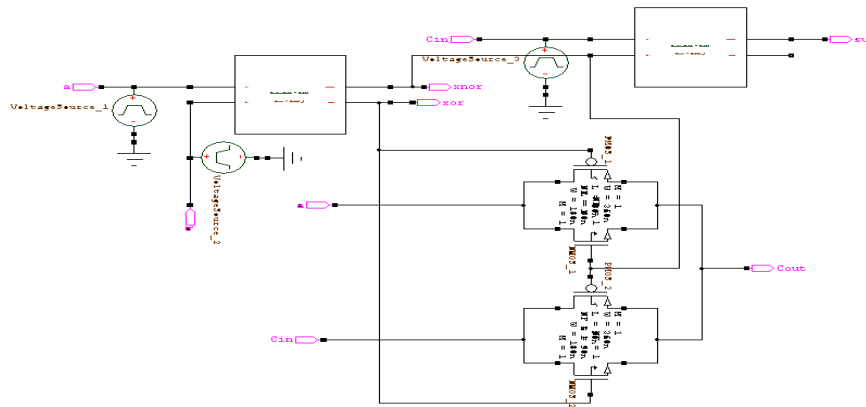


Fig. 6: Full adder using 3 transistor XOR gate.

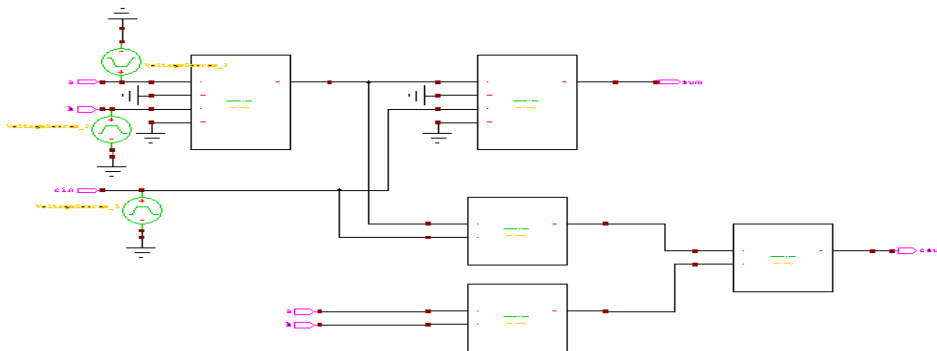


Fig. 7: Full adder using 8 transistor XOR gate.

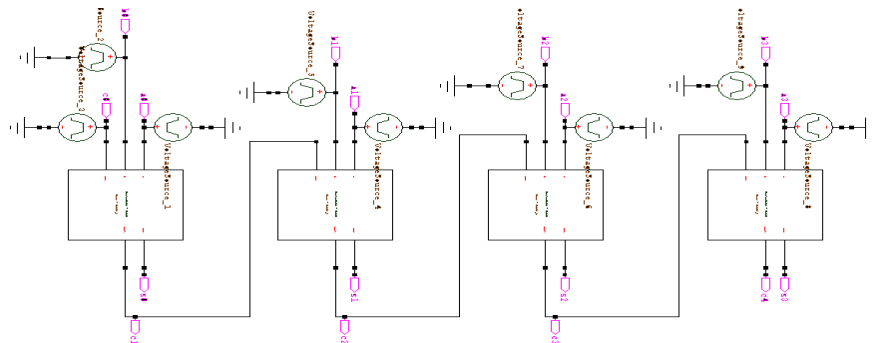


Fig. 8: Schematic for 4-bit RCA with 4 full adders.

D. Carry Skip Adder (CS_{KA}):

The implementation of this adder improves the delay of ripple carry adder. The worst path of carry skip adder begins at the first full adder, passes through all adders and ends at the sum bit. The schematic diagram of carry skip adder is shown in Fig. 12. The simulation output of carry skip adder is shown in Fig. 13.

III. Comparison of Delay of Different Adders:

The 1-bit, 2-bit, 3-bit, 4-bit ripple carry adder, carry select adder and carry skip adder is designed in Tanner and it is simulated by transient analysis. Propagation delay for end to end is obtained by using spice command. The simulation result of adders in terms of delay is shown in TABLE II. The simulation result of adders in term of average power consumed is shown in TABLE III. Comparison of adders in term of delay is shown in Fig.14.

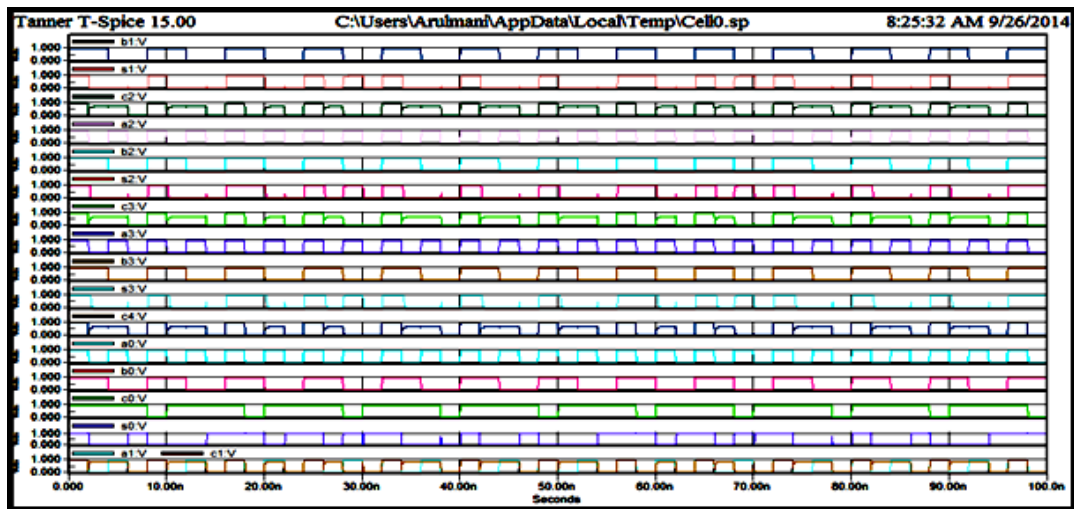


Fig. 9: Simulation output of 4-bit RCA with 4 full adders.

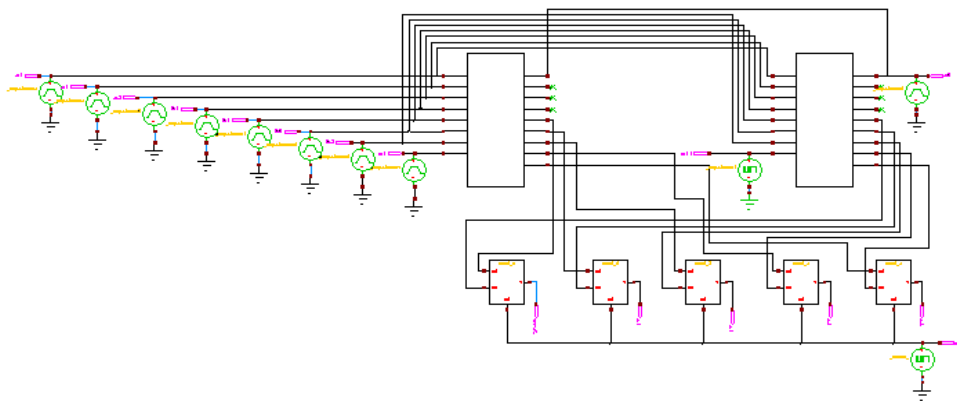


Fig. 10: Schematic diagram of CSA.

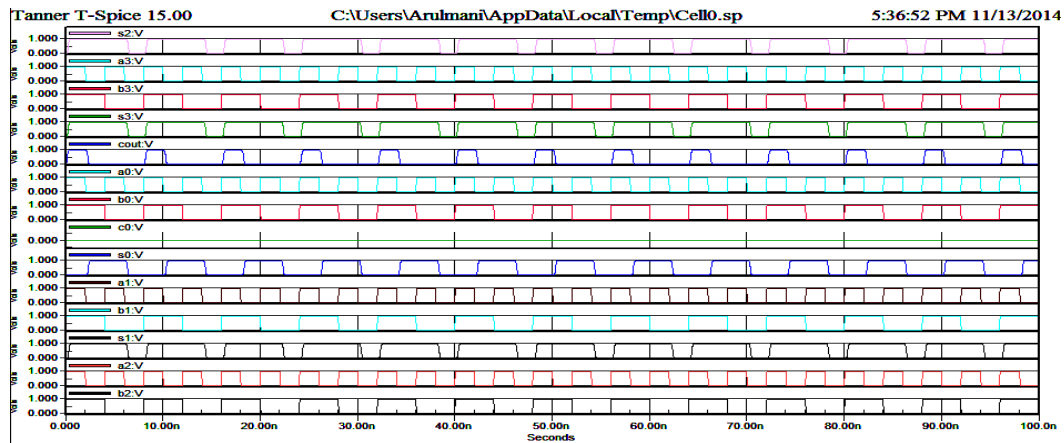


Fig. 11: Simulation output of CSA.

Table II: Delay of ripple carry adder, carry select adder and carry skip adder.

ADDER	DELAY(SEC) USING 8T XOR GATE	DELAY(SEC) USING 3T XOR GATE
1-BIT RCA	4.135n	62.3248p
2-BIT RCA	4.266n	93.4450p
3-BIT RCA	9.174n	132.464p
4-BIT RCA	9.489n	199.9283p
CSA	17.486n	237.9978p
CS _k A	13.22n	61.521p

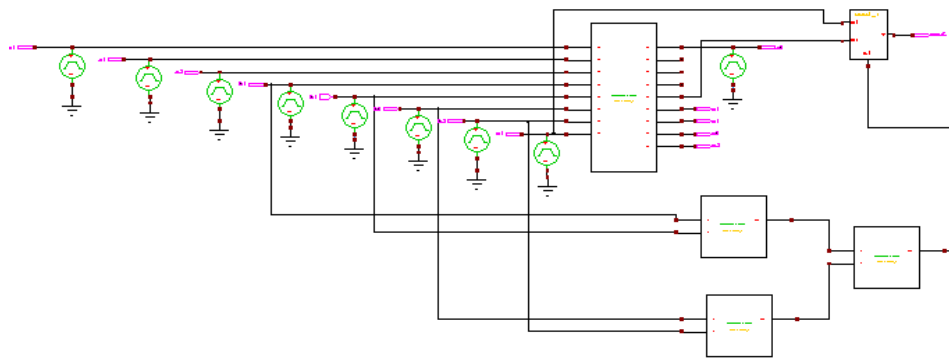


Fig. 12: Schematic diagram of carry skip adder.

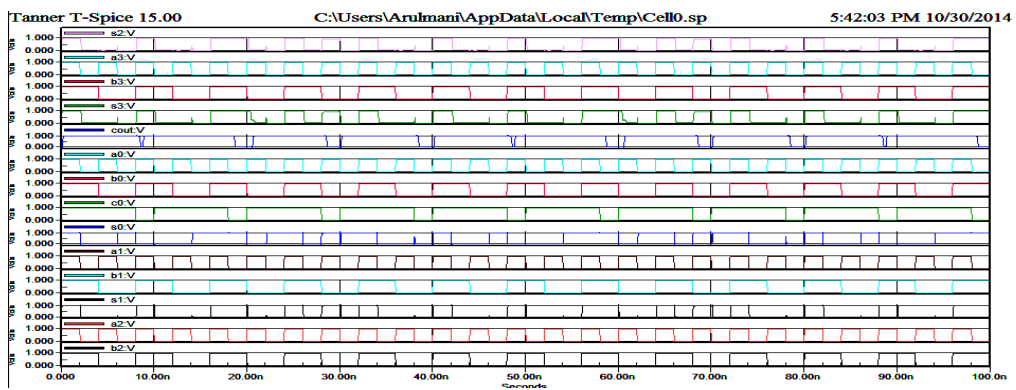


Fig. 13: Simulation output of carry skip adder.

Table III: Average power consumption of ripple carry adder, carry select adder and carry skip adder.

ADDER	AVERAGE POWER (watts) USING 8T XOR GATE	AVERAGE POWER (watts) USING 3T XOR GATE
1-BIT RCA	6.030594e-006	7.080578e-007
2-BIT RCA	6.462637e-006	7.268790e-007
3-BIT RCA	6.967021e-006	7.546914e-007
4-BIT RCA	7.226121e-006	8.340635e-007
CSA	8.569022e-005	9.716521e-006
CS _k A	7.001579e-005	7.246512e-006

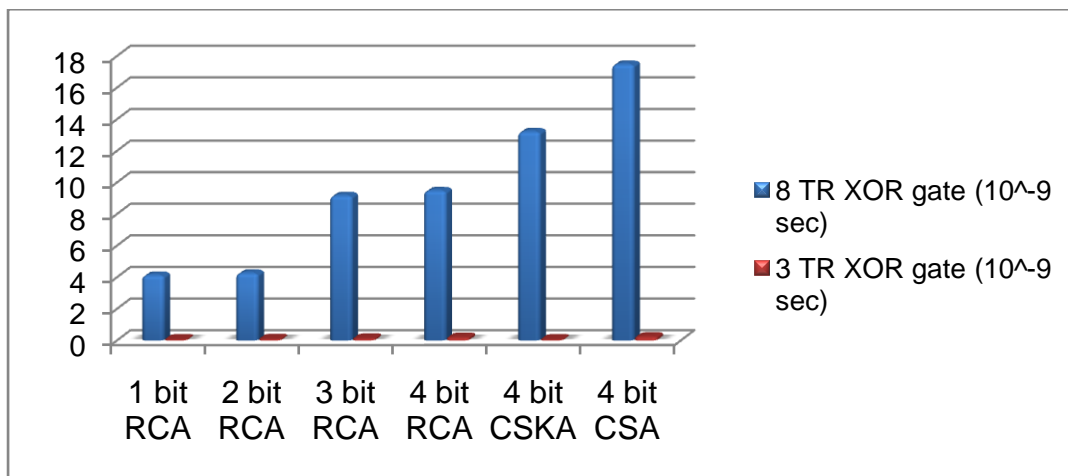


Fig. 14: Comparison of adders in terms of delay.

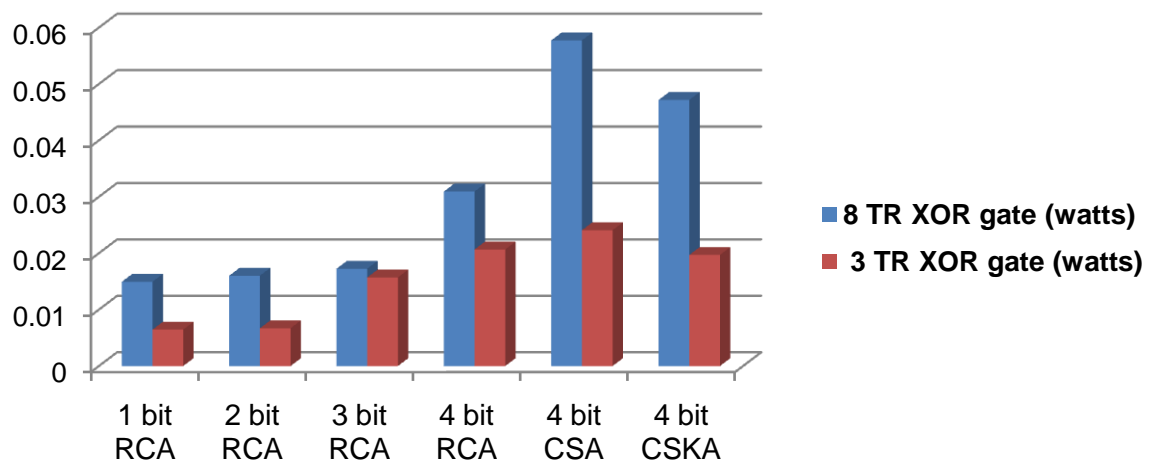


Fig. 15: Comparison of adders in terms of average power consumption.

IV. Conclusion:

In this work, the structure of a ripple carry adder, carry select adder and carry skip adder has been designed using 3 transistor and 8 transistor XOR circuit. The structure of ripple carry adder, carry select adder, carry skip adder has been designed using 3T and 8T XOR in TANNER EDA tool and simulated using 90nm technology. The result shows that delay is lesser in the design using 3T XOR circuit than 8T XOR circuit. As in the theory, the propagation delay of carry skip adder is less than the ripple carry adder.

Zhuang, N. and H. Wu, 1992. "A new design of the CMOS full adder", IEEE J. Solid-State Circuits, 27(5): 840-844.

Zimmermann, R. and W. Fichtner, 1997. "Low-power logic styles: CMOS versus pass-transistor logic", IEEE J. Solid State Circuits, 32(7): 1079-1090.

REFERENCES

Goel, S., A. Kumar and M.A. Bayoumi, 2006. "Design of robust, energy-efficient full adders for deep sub micrometer design using hybrid-CMOS logic style," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 14(12): 1309-1321.

Leblebici, Y. and S.M. Kang, 1999. "CMOS Digital Integrated Circuits", Singapore: Mc Graw Hill, India, 2nd edition.

Muthukumaran, S. and A. Jawahar, 2014. "Design and Performance Analysis of 3 bit ripple carry adder with 14 transistor full adder using Novel 3 transistor XOR gate", Intelligent engineering systems ISBN NO:978-93-83459-33-9.

Shams, A.M. and M. Bayoumi, 2000. "A novel high-performance CMOS 1-bit full adder cell", IEEE Trans. Circuits Syst. II, Analog Digital Signal Process, 47(5): 478-481.

Weste, N. and K. Eshraghian, 1993. "Principles of CMOS VLSI Design, A System Perspective", Addison-Wesley.

Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung, 2004. "A novel multiplexer-based low-power full adder", IEEE Transactions on Circuits and Systems: Express Briefs, 51(7).